Indian Institute of Technology, Kharagpur
Mid-Spring Semester 2017-18

Date of Examination: 22-02-2018 **Session:** AN (2-4 pm) **Duration:** 2 hrs
Subject No.: CS31702
Subject: COMPUTER ARCHITECTURE AND OPERATING SYSTEMS
Department/Center/School: Computer Science and Engineering
Specific charts, graph paper, log book etc., required: NO **Total Marks :** 60
Special instructions (if any): ANSWER ALL QUESTIONS
Note: All parts of the question (a,b,c,d) should be answered at a stretch.

1. (a) Name 8 great ideas exploited extensively by the designers of computer architectures.

   (b) For the following MIPS instructions specify the instruction formats by splitting the 32-bit machine code into subsets and label them. Briefly name the above labels and interpret them in execution of the instruction.

   i. Arithmetic instructions with register operands.
   ii. Arithmetic instructions with immediate operands.
   iii. Memory access instructions
   iv. Branch instructions
   v. Jump instructions

   (c) Write the MIPS code for the following C function. Provide suitable comments against to each MIPS instruction for understanding its functionality.

```
int sum(int a, int b, int c, int d)
{
int e;
e = a+b+c+d;
return(e);
}
```

   (d) Answer the following in view of IEEE 754 Single precesion floating point number representation:

   i. Representation format with appropriate details (number of bits and labels associated to different subsets).
   ii. How the floating point value is computed from the above representation?
   iii. Compute the range of numbers that can be represented using single precesion encoding.

   (2+10+5+3 = 20M)

2. (a) Discuss how combinational and sequential logics differ? Provide 2 example circuits to each of the logic.

   (b) Design data path and controller for a single-cycle processor to execute R-type, memory reference and control flow instructions. Draw a neat sketch with all hardware components and place the connections and signals carefully. Highlight the salient points in the design of above mentioned datapath and controller.

(c) How a multi-cycle processor (without pipelining) differ from single-cycle processor? Mention its advantages as well as disadvantages over single-cycle processor?

(d) Mention the additional functional units (hardware) and modifications in the datapath of a 5-stage multi-cycle pipeline processor (assume there is no need to address hazards), when compared with the datapath of single-cycle processor in executing R-type, memory reference and control flow instructions.

(2+8+2+3 = 15M)

3. (a) Discuss the core reasons for structural, data and contorl hazards in case of pipeline processors. Suggest the strategies to minimise the effect of the above hazards to improve the efficiency of pipeline processor. Provide more details in case of compensating the data and control hazards.

(b) Illustrate the flow of the following sequence of instructions through 5-stage multi-cycle pipeline processor using suitable diagrams synchronized to clock.

lw s2, 40(s1)
add s3, s2, s4
or s5, s2, s6
and s7, s5, s3

Clearly show and explain (in sequence w.r.t clock) the sequence of events (hazards) occur and actions taken against to the hazards in view of execution of the above sequence of instructions.

(c) How the pipeline stalls will be implemented?

(5+8+2 = 15M)

4. (a) Briefly explain the following (in the context of memory access through memory hierarchy):

i. Compulsory miss & its solution
ii. Capacity miss & its solution
iii. Conflict miss & its solution
iv. Write-through policy
v. Write-back policy

(b) Design a set-associative cache for the following specifications: (i) size of main memory = 16 MB, (ii) size of cache (only data) = 64 KB, (iii) block size = 64 bytes and (iv) number of sets = 512. Here, CPU access data at word level. Show the hardware implementation of the cache for the above specifications. Mention the following details in view of the above set-associative cache:

i. Size of the Tag field
ii. In the context of n-way associative, what is the value of "n" in this problem?
iii. What is the total size of the cache including the overhead?

(5+5 = 10M)