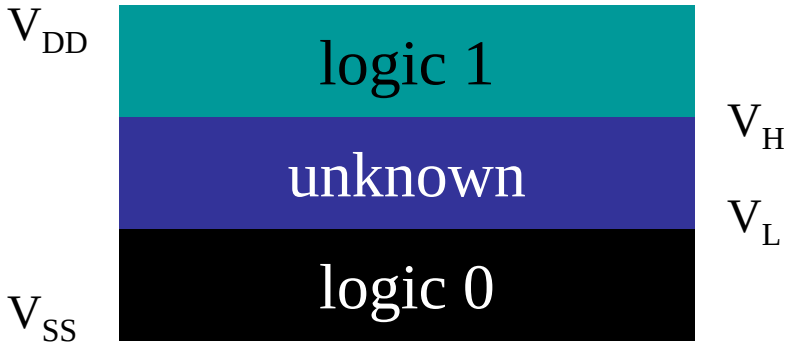
Noise Margin and Gate Delay

Debdeep Mukhpadhyay

IIT Madras

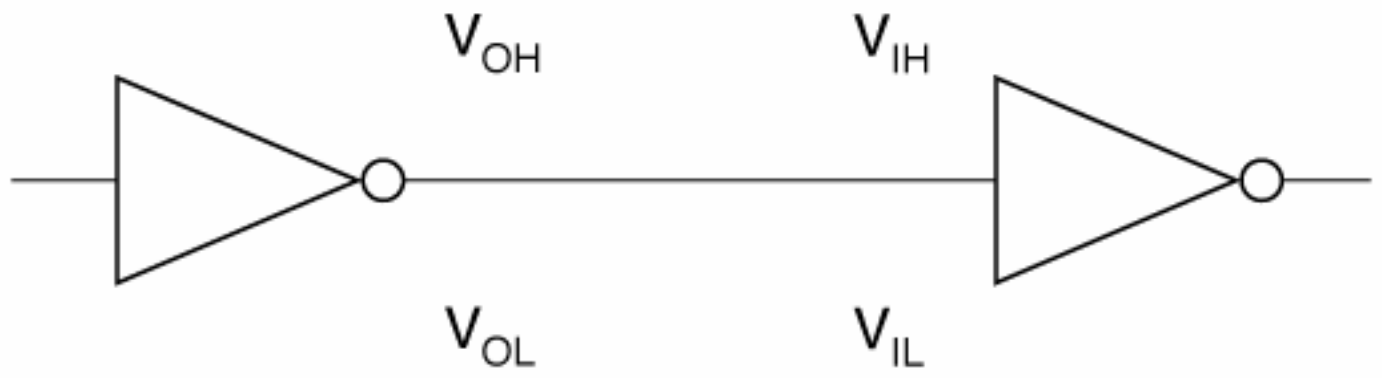
Logic levels

- Solid logic 0/1 defined by V_{SS}/V_{DD}.
- Inner bounds of logic values V_L/V_H are not directly determined by circuit properties, as in some other logic families.



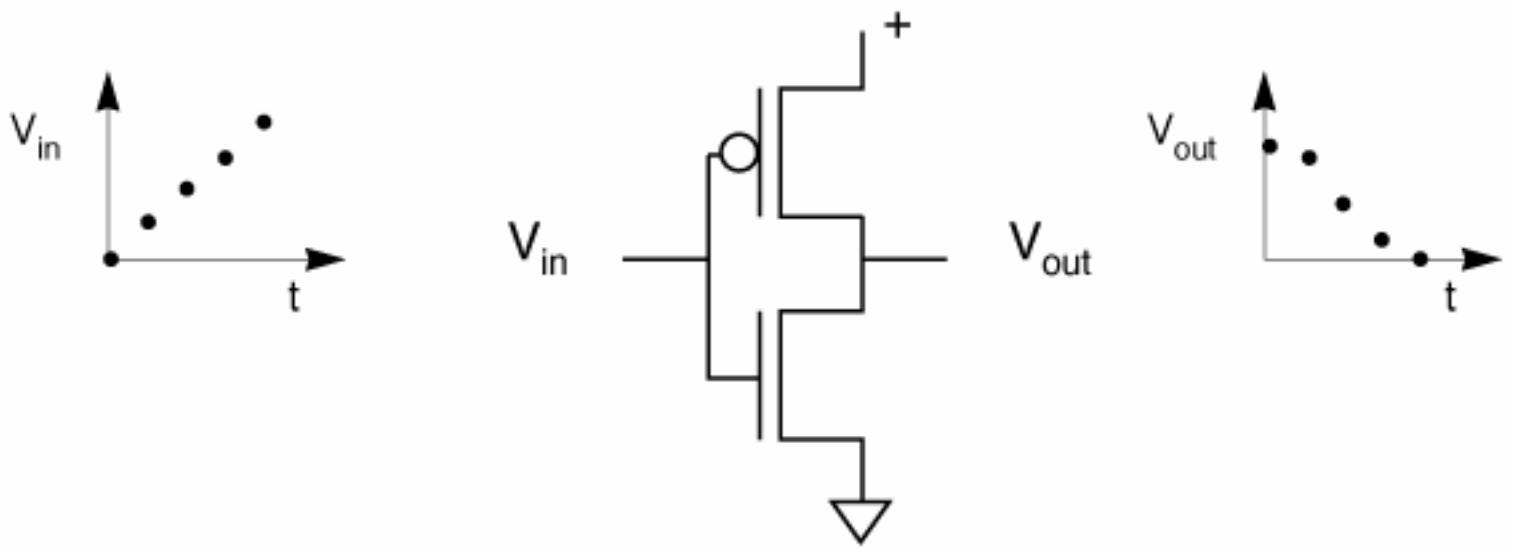
Logic level matching

- Levels at output of one gate must be sufficient to drive next gate.



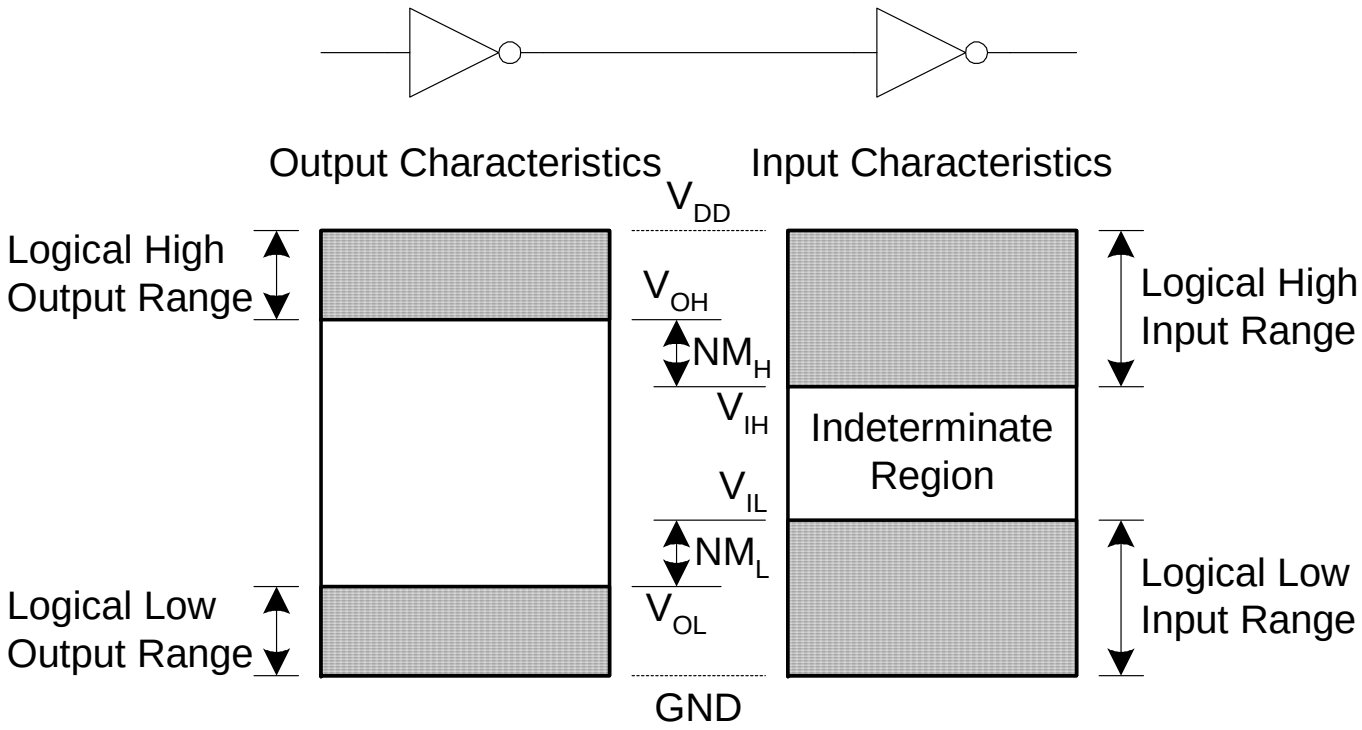
Transfer characteristics

- Transfer curve shows static input/output relationship—hold input voltage, measure output voltage.



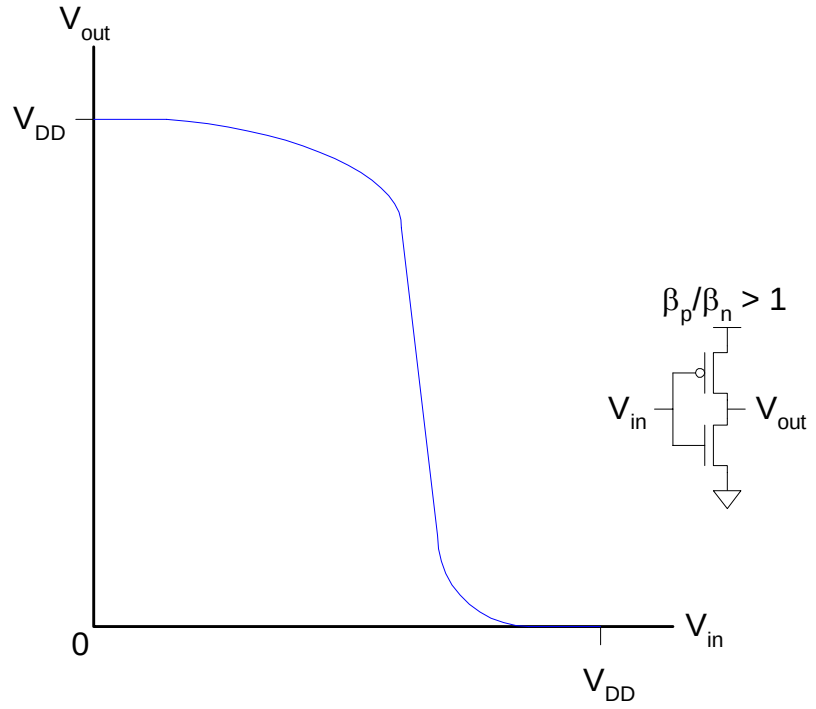
Noise Margins

- How much noise can a gate input see before it does not recognize the input?



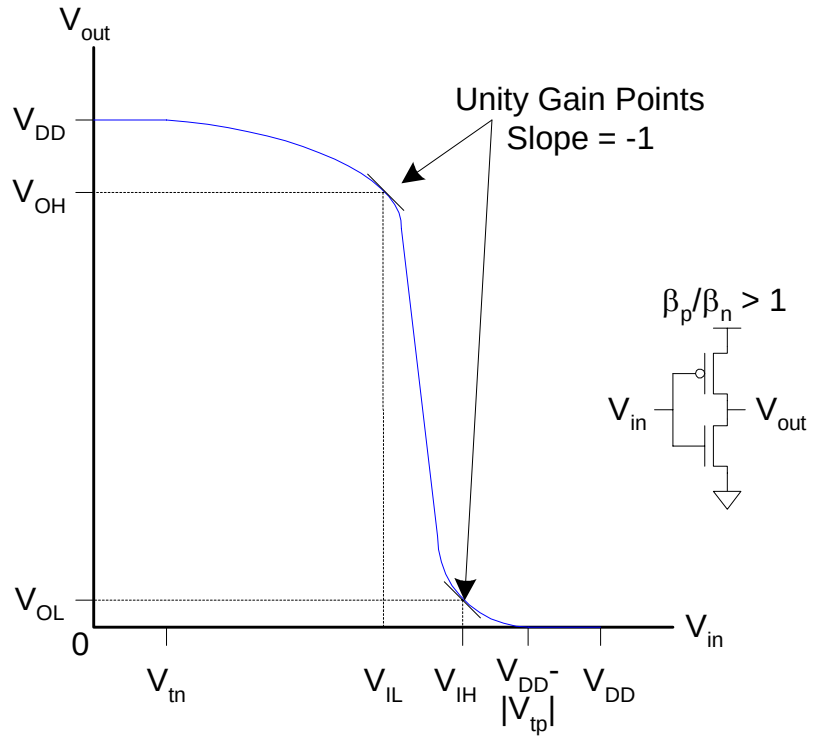
Logic Levels

- To maximize noise margins, select logic levels at



Logic Levels

- To maximize noise margins, select logic levels at
  - unity gain point of DC transfer characteristic



Noise margin

- Noise margin = voltage difference between output of one gate and input of next. Noise must exceed noise margin to make second gate produce wrong output.

Delay Definitions

- $\mathbf{t_{pdr}}$:
- $\mathbf{t_{pdf}}$:
- $\mathbf{t_{pd}}$:
- $\mathbf{t_{r}}$:
- $\mathbf{t_{f}}$: *fall time*

Delay Definitions

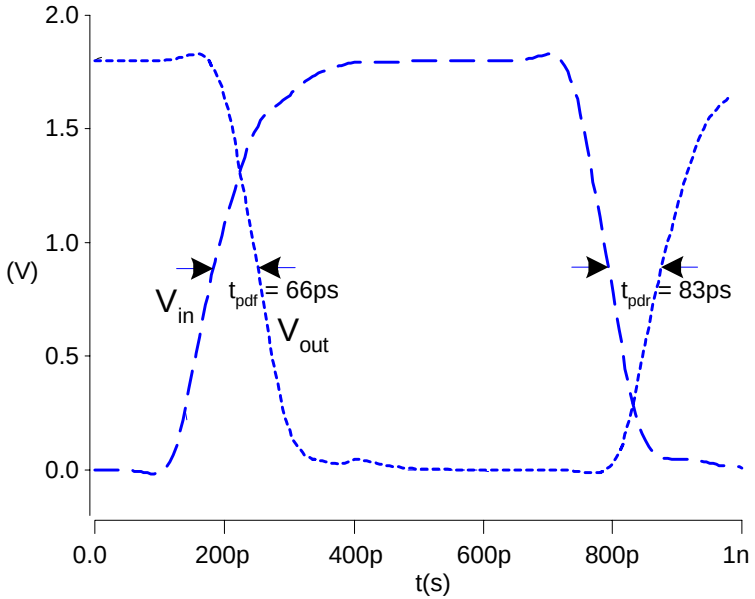
- **t_{pdr}**: *rising propagation delay*
  - From input to rising output crossing $V_{DD}/2$
- **t_{pdf}**: *falling propagation delay*
  - From input to falling output crossing $V_{DD}/2$
- **t_{pd}**: *average propagation delay*
  - $t_{pd} = (t_{pdr} + t_{pdf})/2$
- **t_r**: *rise time*
  - From output crossing 0.2 V_{DD} to 0.8 V_{DD}
- **t_f**: *fall time*
  - From output crossing 0.8 V_{DD} to 0.2 V_{DD}

Delay Definitions

- **t_{cdr}**: *rising contamination delay*
  - From input to rising output crossing $V_{DD}/2$
- **t_{cdf}**: *falling contamination delay*
  - From input to falling output crossing $V_{DD}/2$
- **t_{cd}**: *average contamination delay*
  - $t_{pd} = (t_{cdr} + t_{cdf})/2$

Simulated Inverter Delay

- Solving differential equations by hand is too hard
- SPICE simulator solves the equations numerically
  - Uses more accurate I-V models too!
- But simulations take time to write

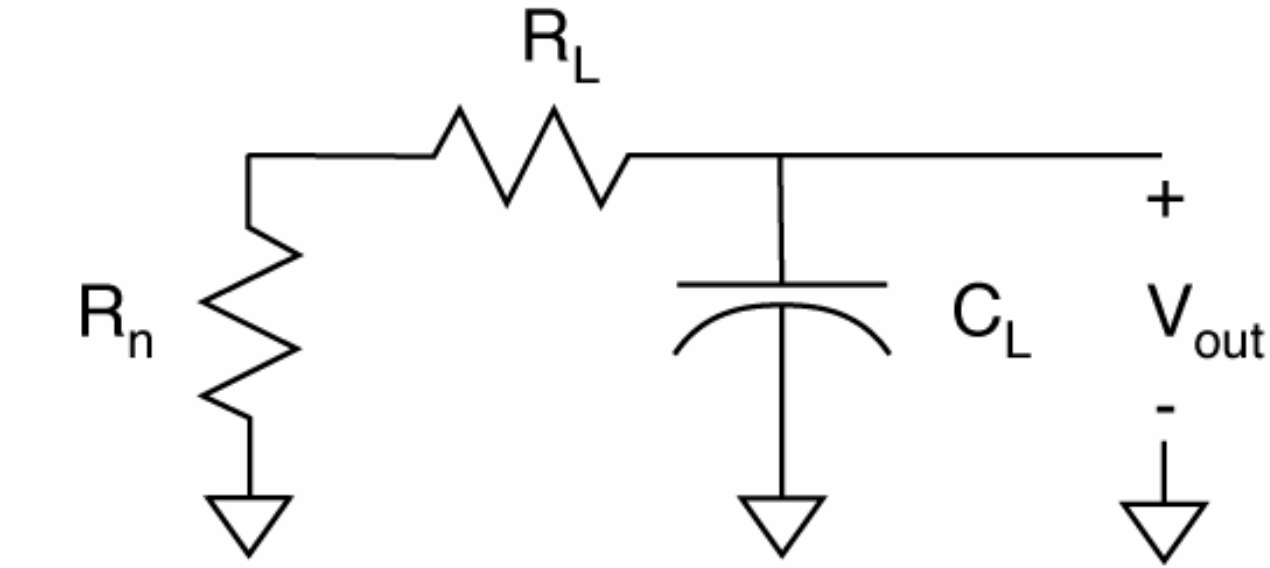


Delay Estimation

- We would like to be able to easily estimate delay
  - Not as accurate as simulation
  - But can we give estimates?
- The step response usually looks like a 1st order RC response with a decaying exponential.
- Use RC delay models to estimate delay
  - C = total capacitance on output node
  - Use *effective resistance* R
  - So that t_{pd} = RC
- Characterize transistors by finding their effective R
  - Depends on average current as gate switches

RC delay

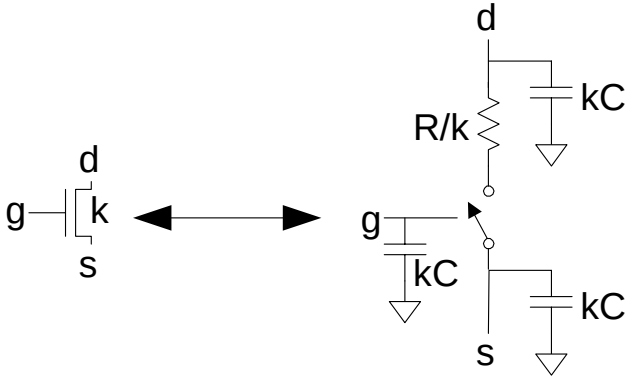
- Load is resistor + capacitor, driver is resistor.

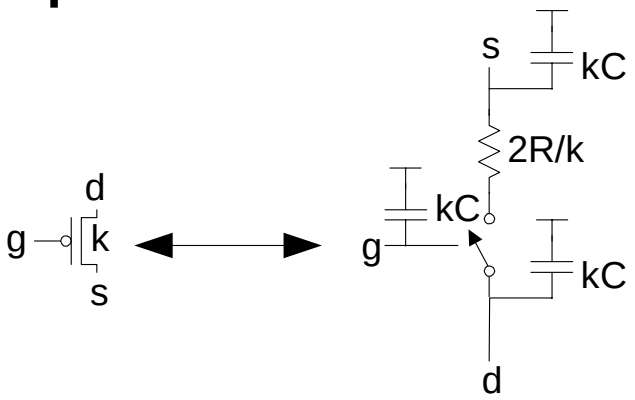


- tf = 0.69 R CL
- For rise time replace by the PMOS resistance.

RC Delay Models

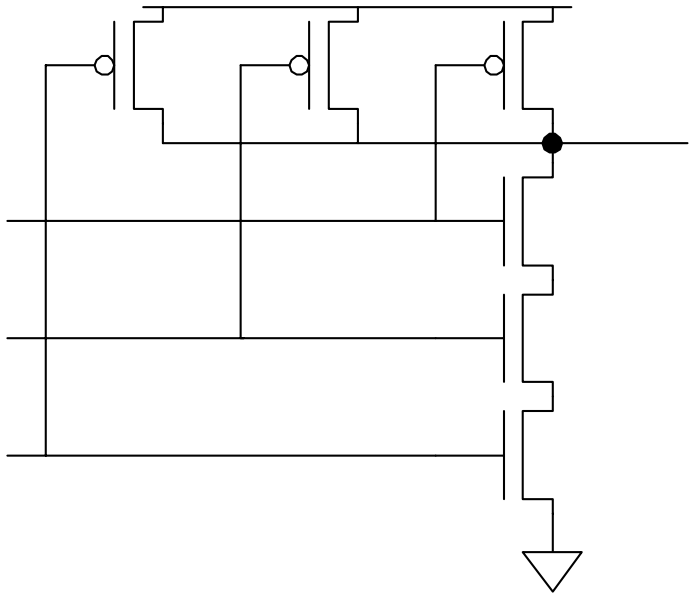
- Use equivalent circuits for MOS transistors
  - Ideal switch + capacitance and ON resistance
  - Unit nMOS has resistance R, capacitance C
  - Unit pMOS has resistance 2R, capacitance C
- Capacitance proportional to width
- Resistance inversely proportional to width





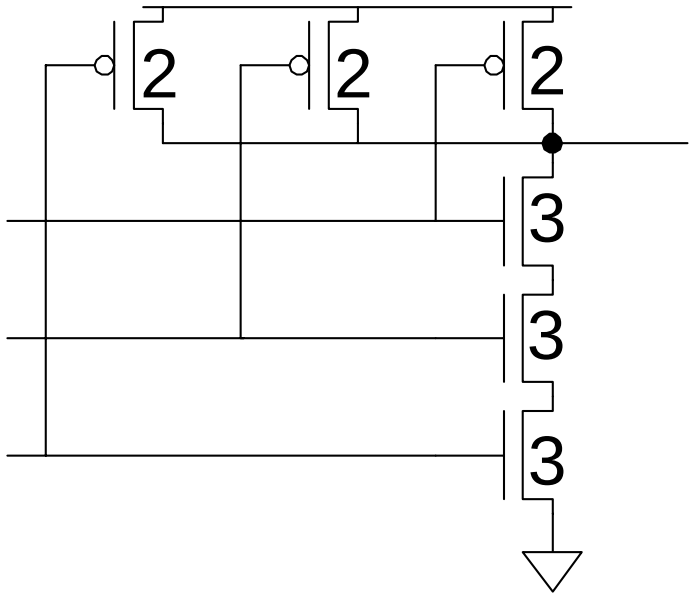
Example: 3-input NAND

- Sketch a 3-input NAND with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).



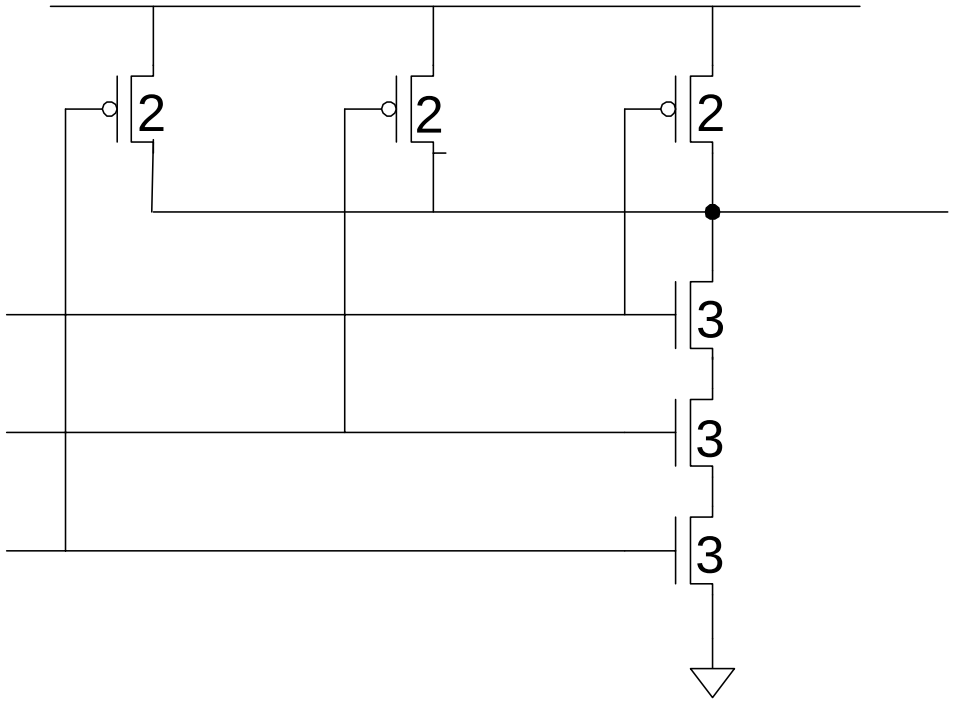
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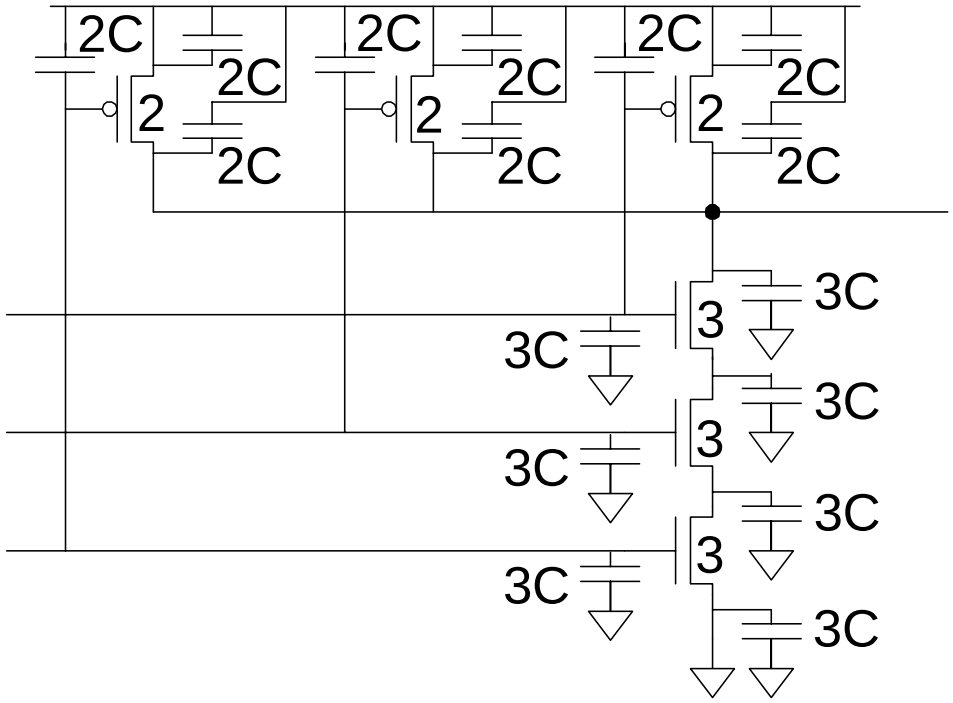
3-input NAND Caps

- Annotate the 3-input NAND gate with gate and diffusion capacitance.



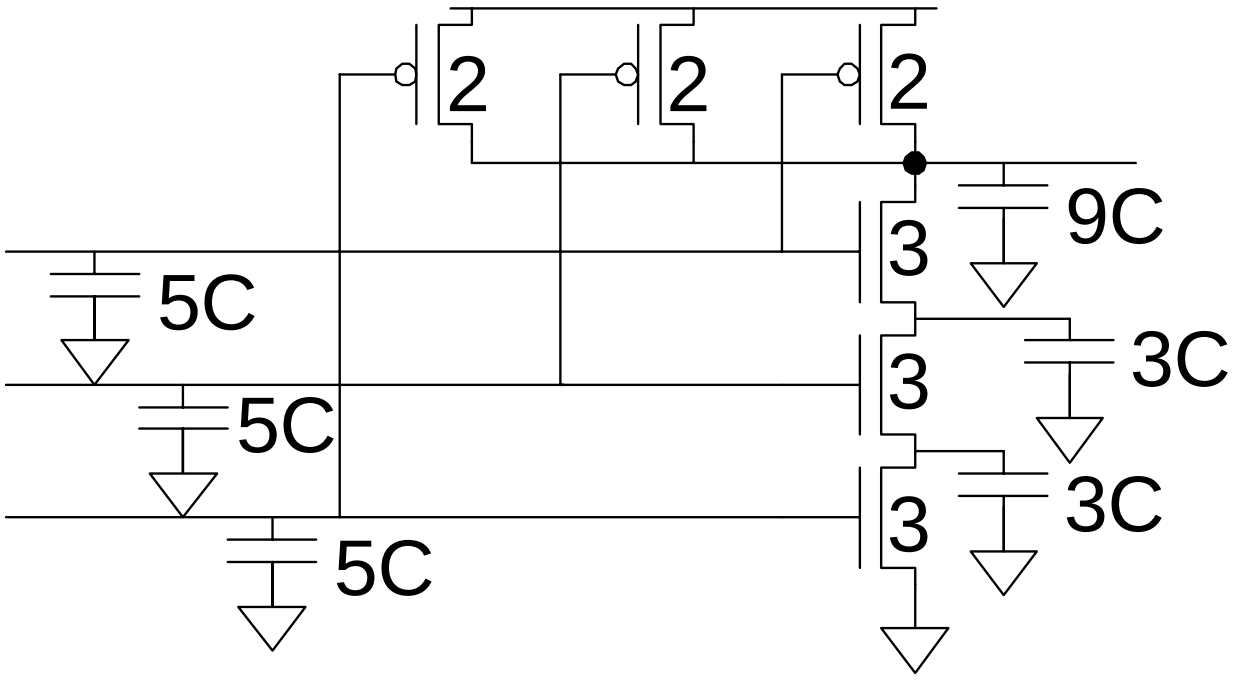
3-input NAND Capacitors

- Annotate the 3-input NAND gate with gate and diffusion capacitance.



3-input NAND Capacitors

- Annotate the 3-input NAND gate with gate and diffusion capacitance.

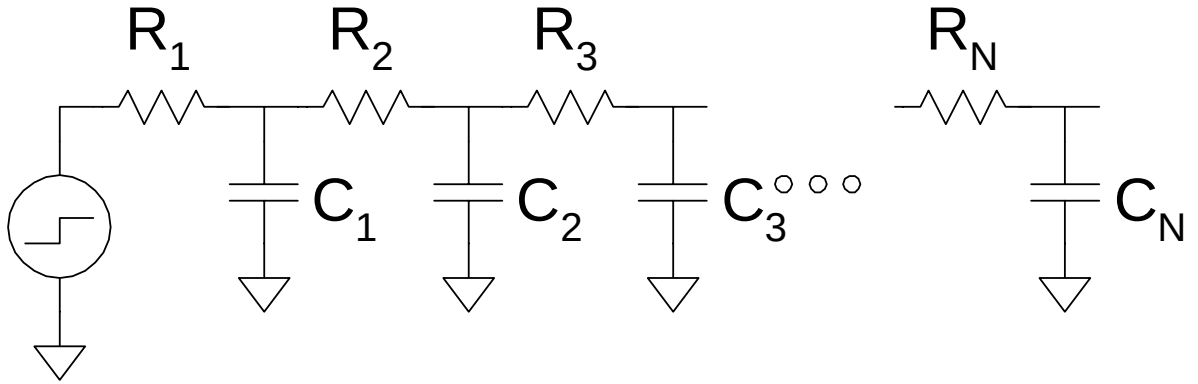


Elmore Delay

- ON transistors look like resistors
- Pullup or pulldown network modeled as *RC ladder*
- Elmore delay of RC ladder

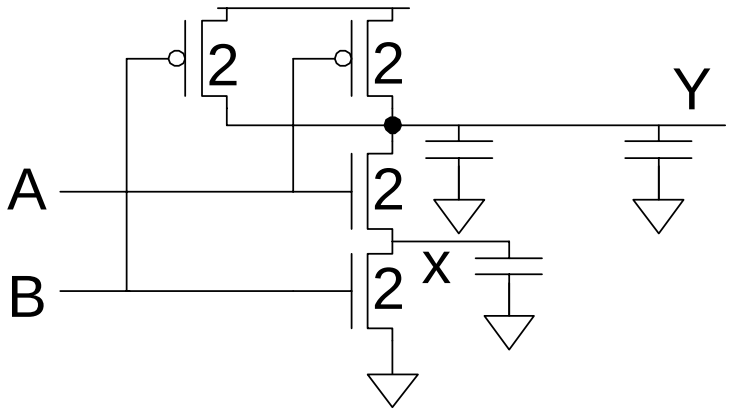
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

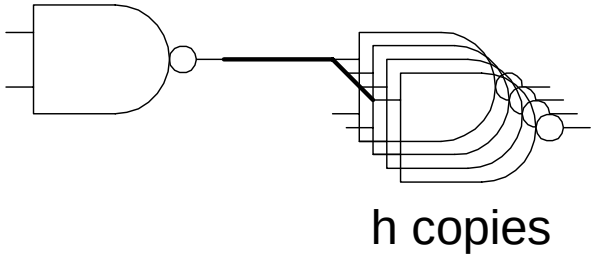
$$= R_1 C_1 + \left(R_1 + R_2\right) C_2 + \ldots + \left(R_1 + R_2 + \ldots + R_N\right) C_N$$



Example: 2-input NAND

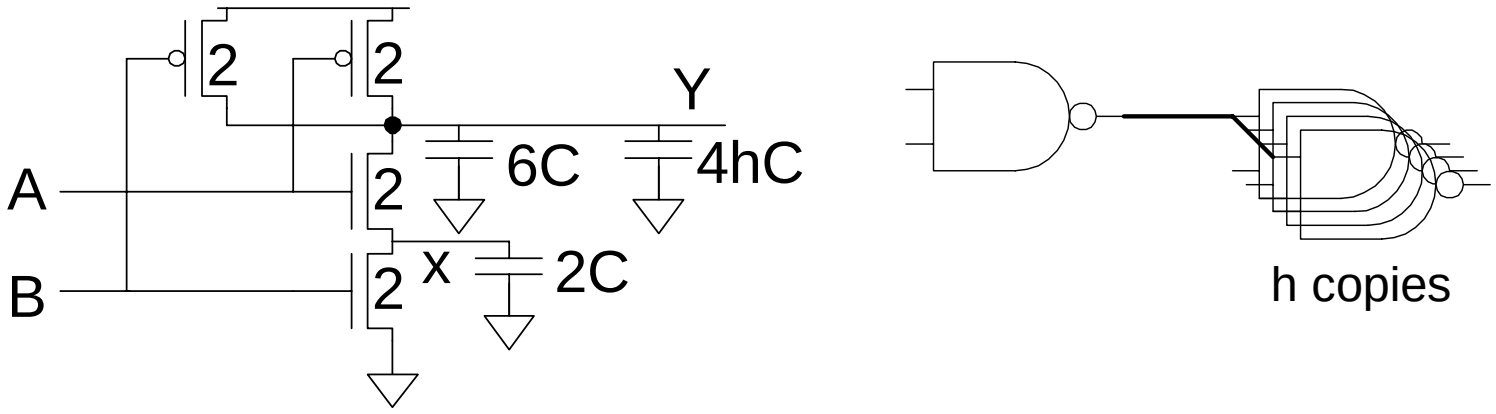
- Estimate worst-case rising and falling delay of 2-input NAND driving *h* identical gates.





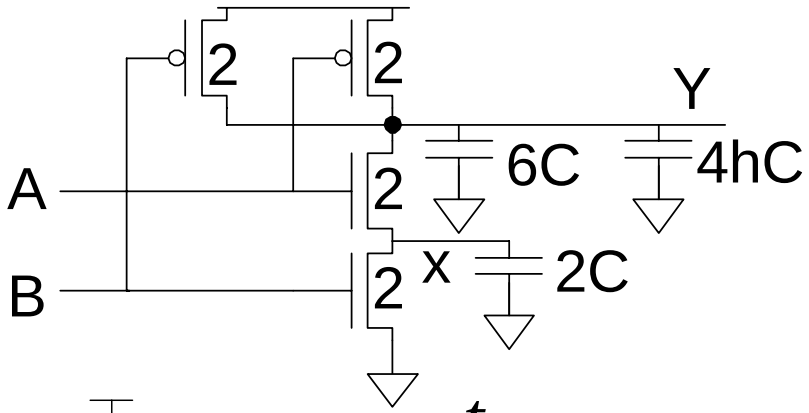
Example: 2-input NAND

- Estimate rising and falling propagation delays of a 2-input NAND driving *h* identical gates.

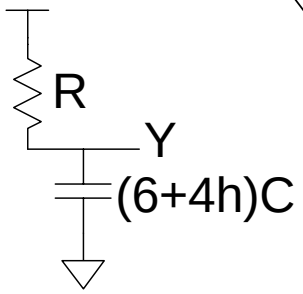


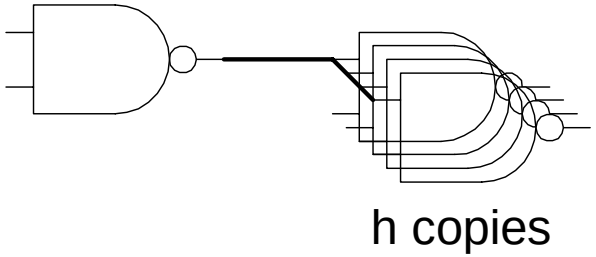
Example: 2-input NAND

- Estimate rising and falling propagation delays of a 2-input NAND driving *h* identical gates.



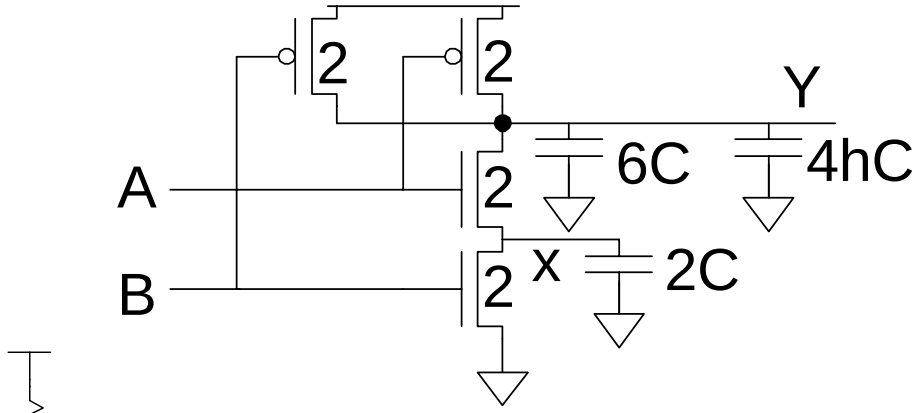
$t_{pdr} =$

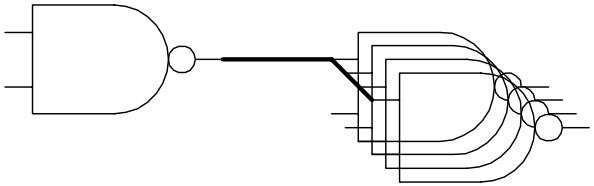




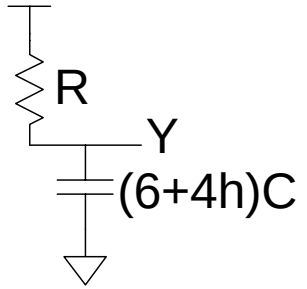
Example: 2-input NAND

- Estimate rising and falling propagation delays of a 2-input NAND driving *h* identical gates.





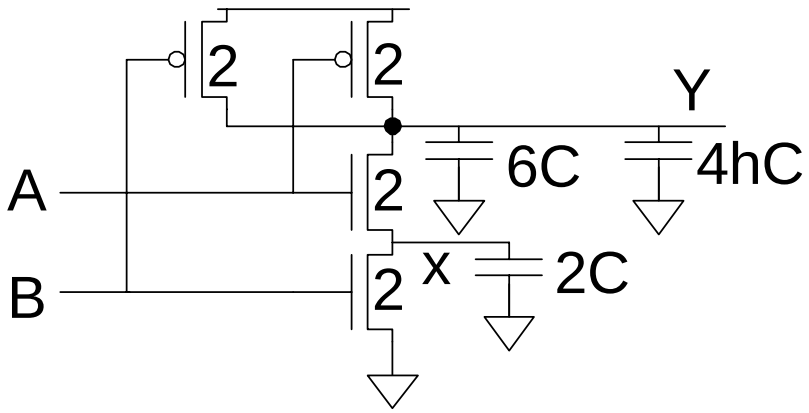
h copies

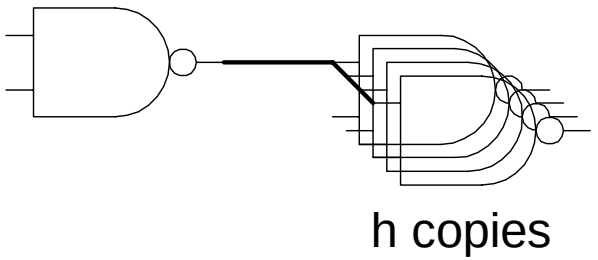


$$t_{pdr} = \left(6 + 4h\right) RC$$

Example: 2-input NAND

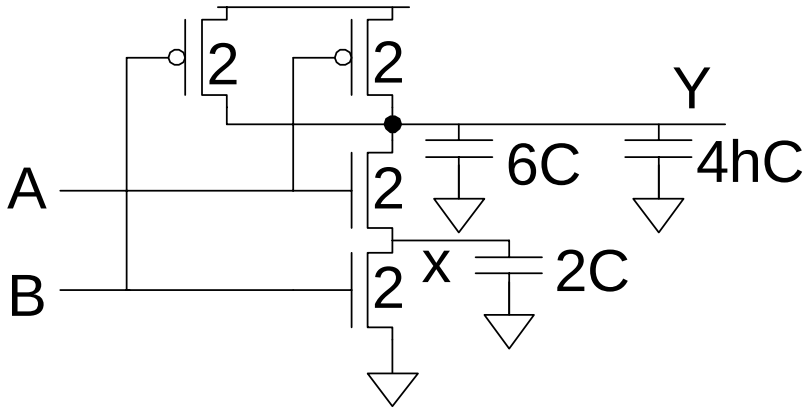
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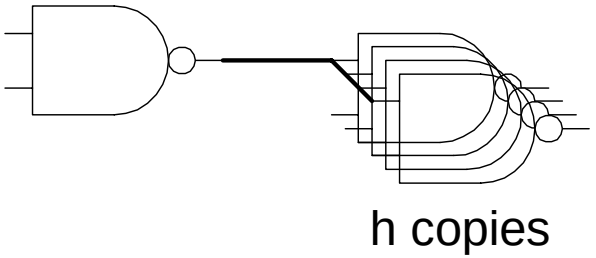


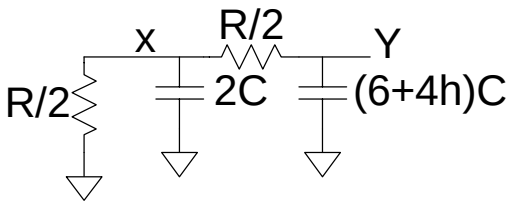


Example: 2-input NAND

- Estimate rising and falling propagation delays of a 2-input NAND driving *h* identical gates.



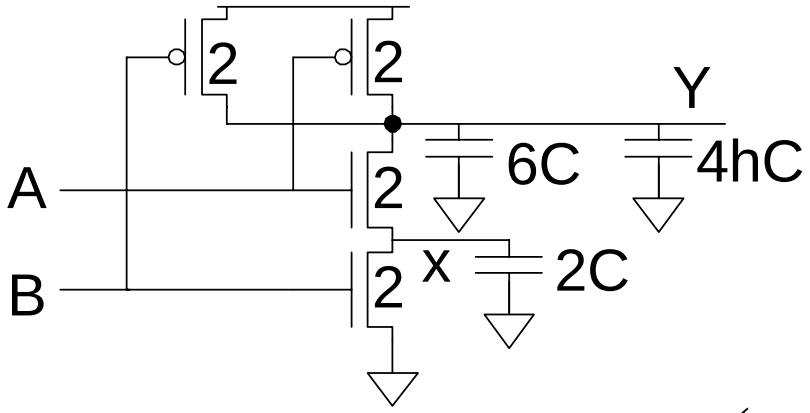


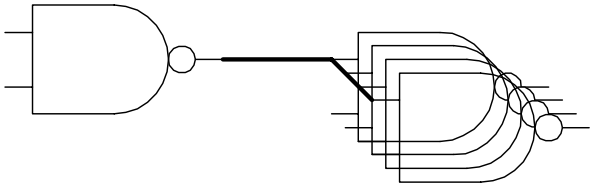


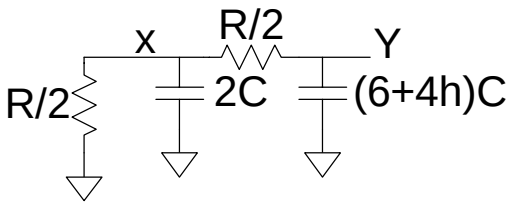
$$t_{pdf} =$$

Example: 2-input NAND

- Estimate rising and falling propagation delays of a 2-input NAND driving *h* identical gates.







$$t_{pdf} = (2C)\left(\frac{R}{2}\right) + \left[(6+4h)C\right]\left(\frac{R}{2}+\frac{R}{2}\right)$$

$$= (7+4h)RC$$

Delay Components

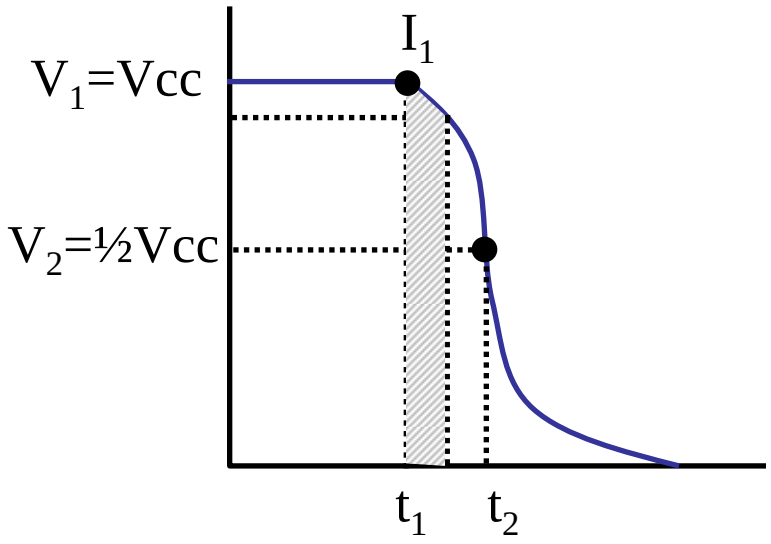
- Delay has two parts
  - *Parasitic delay*
    - 6 or 7 RC
    - Independent of load
  - *Effort delay*
    - 4h RC
    - Proportional to load capacitance

CMOS inverter delay

- An approximate method:
  - Assume constant I_{avg}
  - The NMOS and the PMOS are in saturated region and provide a constant current.

$$t_{PHL} = \frac{C_{load} V_{CC}}{k_n \left(V_{CC} - V_{Tn}\right)^2}$$

$$t_{PLH} = \frac{C_{load} V_{CC}}{k_p \left(V_{CC} - \left|V_{TP}\right|\right)^2}$$



$$I_{avg} = I_1$$

Some Points

- The delay of a gate, be it the rise or the fall time is inversely proportional to VDD.
- Point to ponder: Effect of sizing on the inverter gate delay.