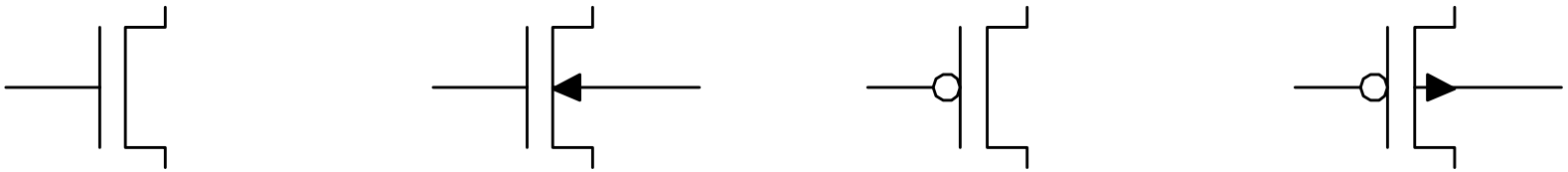
The MOS Transistor

Debdeep Mukhopadhyay

IIT Madras

Introduction

- So far, we have treated transistors as ideal switches
- An ON transistor passes a finite amount of current
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitance
  - $I = C (\Delta V/\Delta t) \rightarrow \Delta t = (C/I) \Delta V$
  - Capacitance and current determine speed
- Also explore what a “degraded level” really means

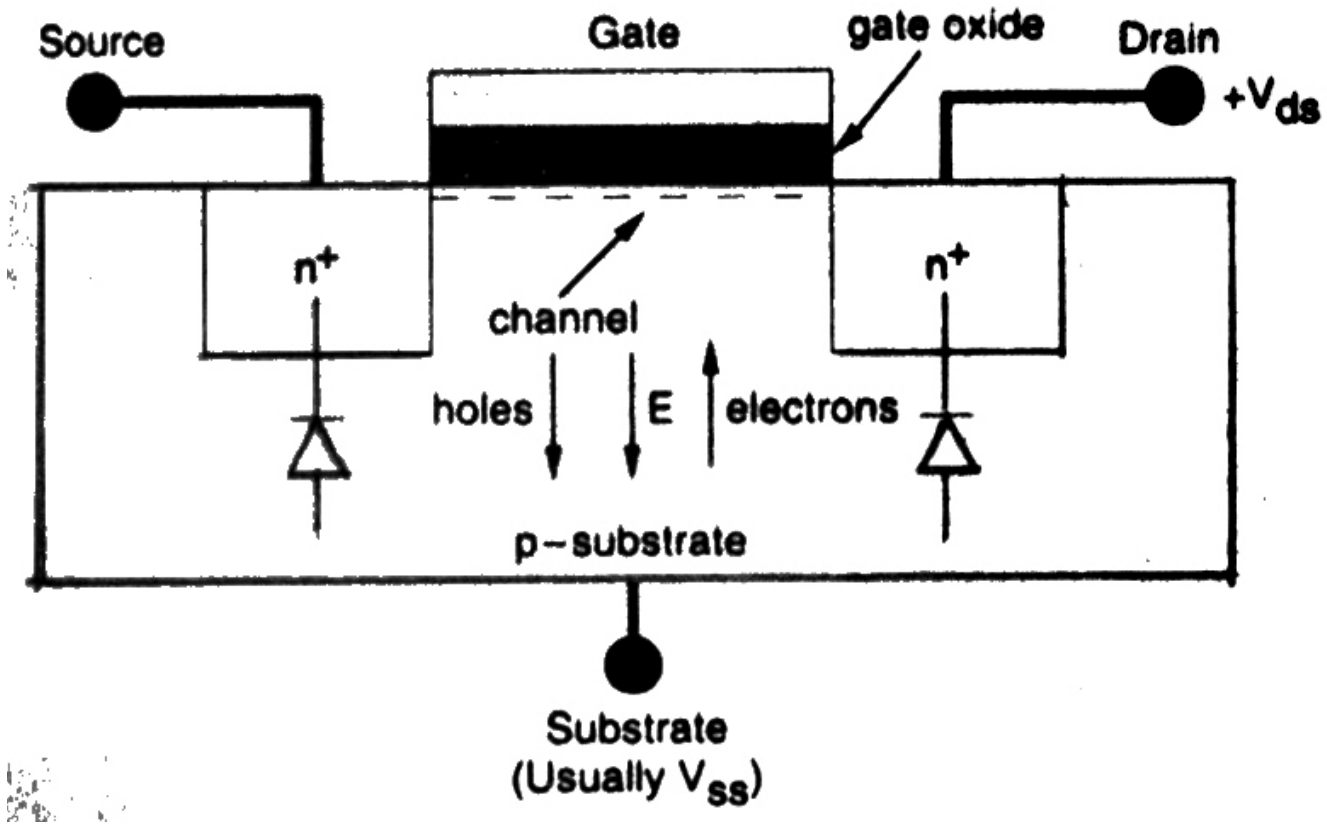


MOS Characteristics

- MOS – majority carrier device
- Carriers: e^{--} in *n*MOS, holes in *p*MOS
- V_t – channel threshold voltage (cuts off for voltages $< V_t$)

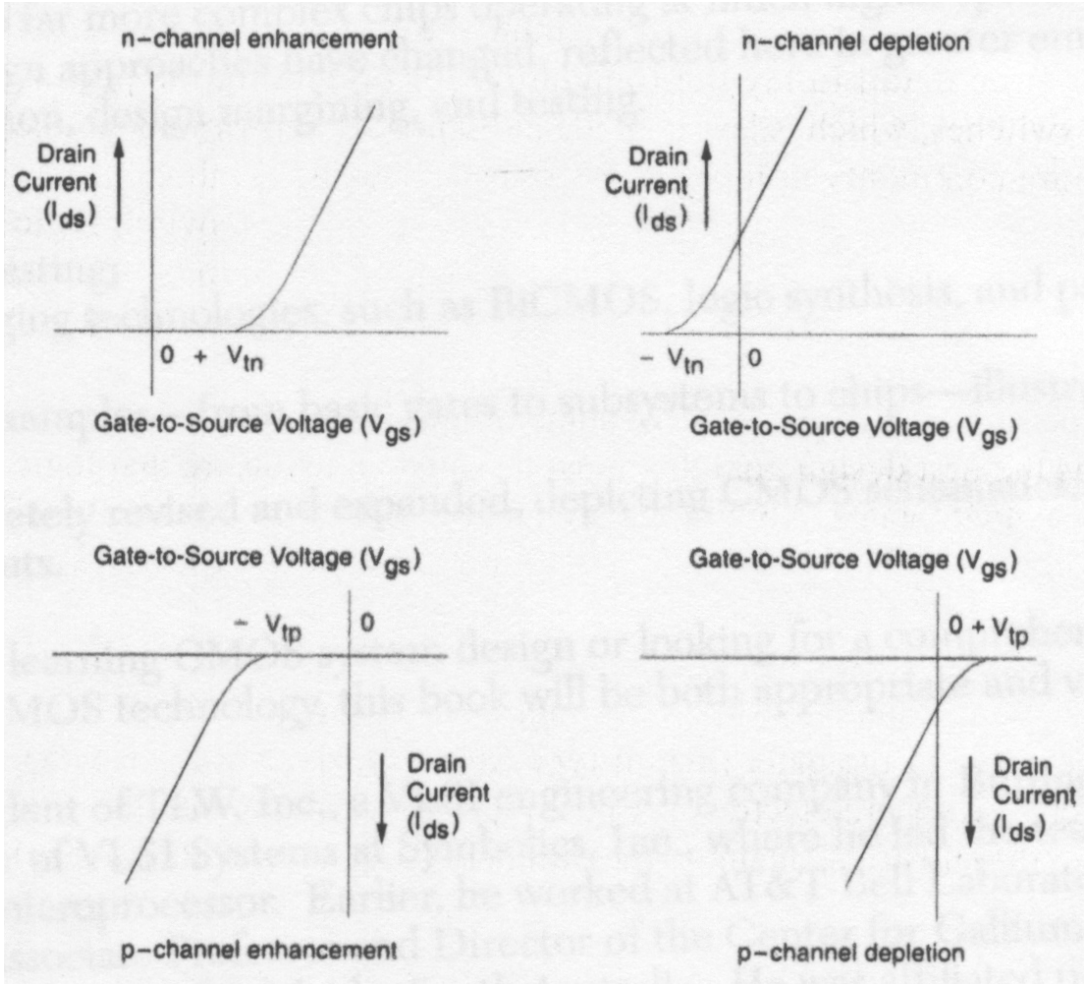
*n*MOS Enhancement Transistor

- Moderately doped *p* type Si substrate
- 2 Heavily doped n^+ regions



I vs. V Plots

- *Enhancement* and *depletion* transistors
  - CMOS – uses only enhancement transistors
  - *n*MOS – uses both



Materials and Dopants

- SiO_2 – low loss, high dielectric strength
  - High gate fields are possible
- *n* type impurities: P, As, Sb
- *p* type impurities: B, Al, Ga, In

Bipolar vs. MOS

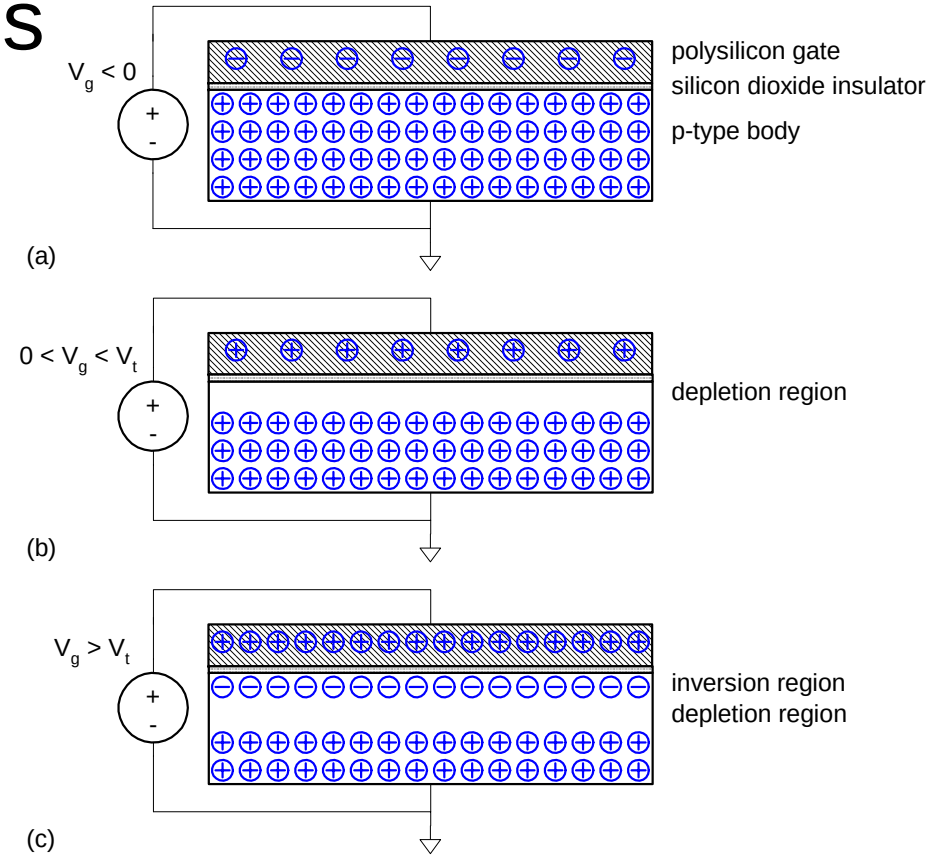
- Bipolar – *p-n* junction – metallurgical
- MOS
  - Inversion layer / substrate junction field-induced
  - Voltage-controlled switch, conducts when $V_{gs} \geq V_t$
  - e^{--} swept along channel when $V_{ds} > 0$ by horizontal component of $\vec{E}$
  - Pinch-off – conduction by e^{--} drift mechanism caused by positive drain voltage
  - Pinched-off channel voltage: $V_{gs} - V_t$ (saturated)
  - Reverse-biased *p-n* junction insulates from the substrate

MOSFET Transistors

- MOSFET – For given V_{ds} & V_{gs}, I_{ds} controlled by:
  - Distance between source & drain L
  - Channel width W
  - Threshold Voltage V_t
  - Gate oxide thickness t_{ox}
  - dielectric constant of gate oxide ε
  - Carrier mobility μ

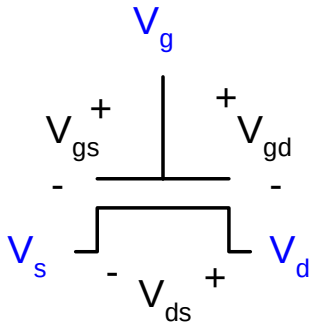
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion



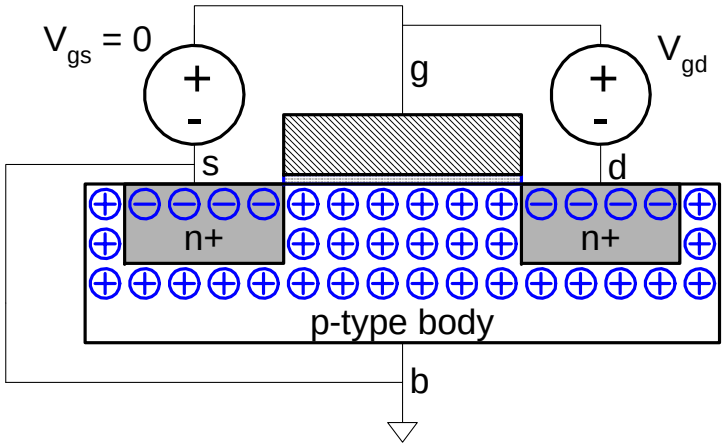
Terminal Voltages

- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*



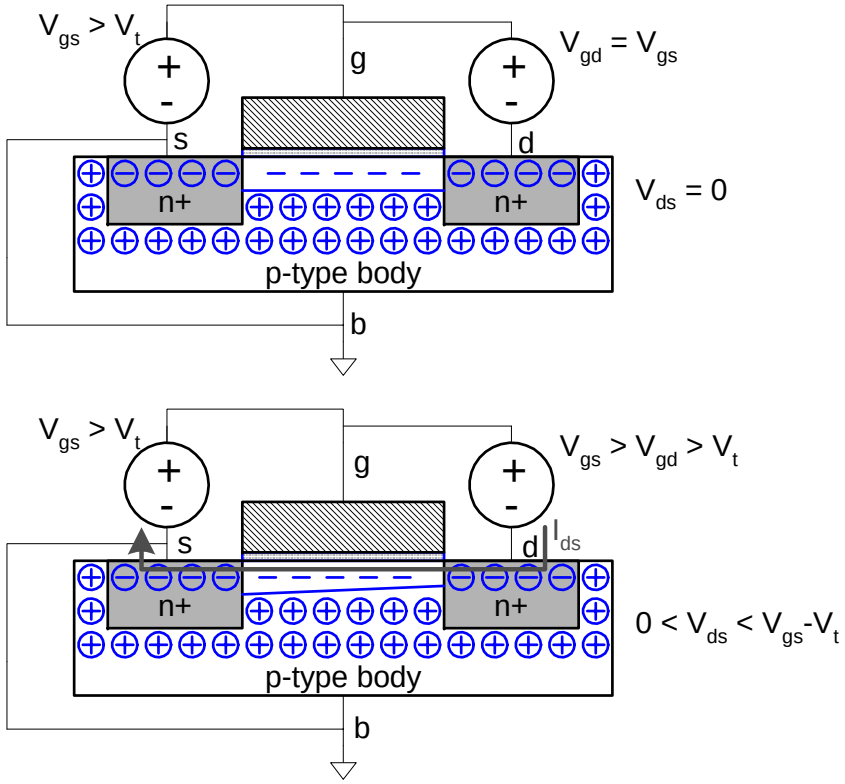
*n*MOS Cutoff

- No channel
- $I_{ds} = 0$



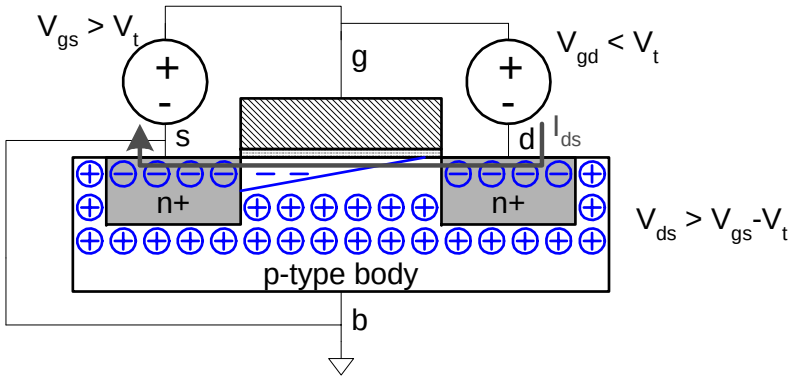
*n*MOS Linear

- Channel forms
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor
- At drain end of channel, only difference between gate & drain voltages effective for channel creation



*n*MOS Saturation

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current saturates
- Similar to current source

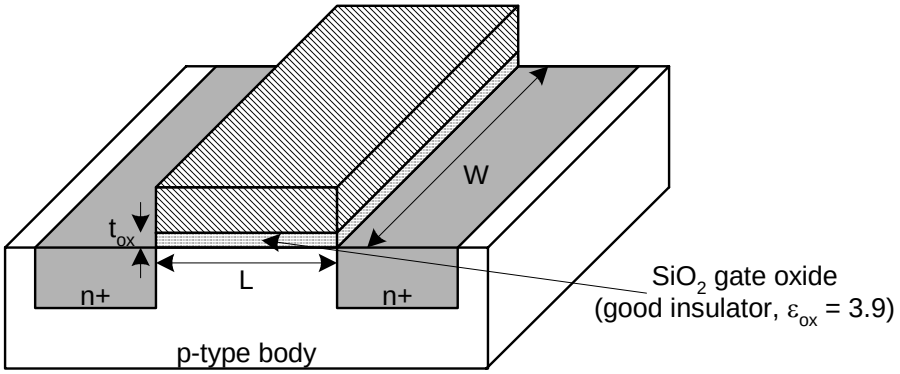


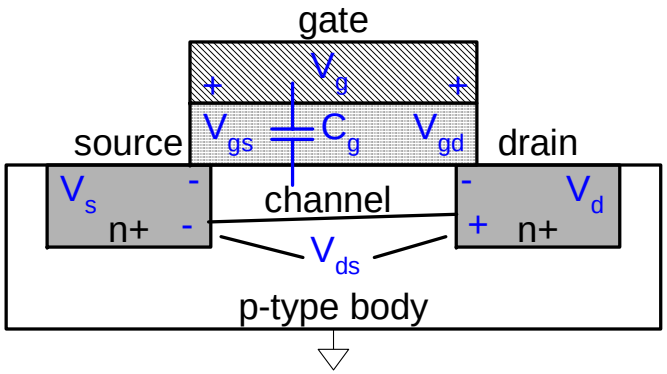
I-V Characteristics

- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

Channel Charge

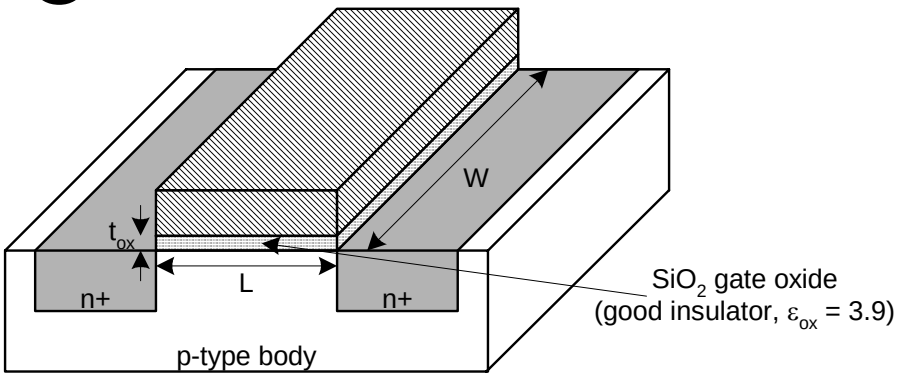
- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel}$ =

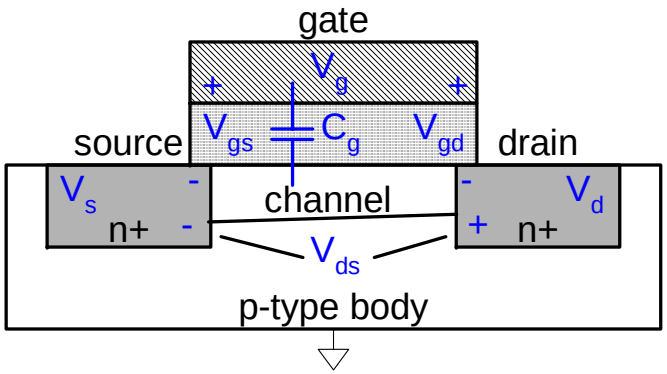




Channel Charge

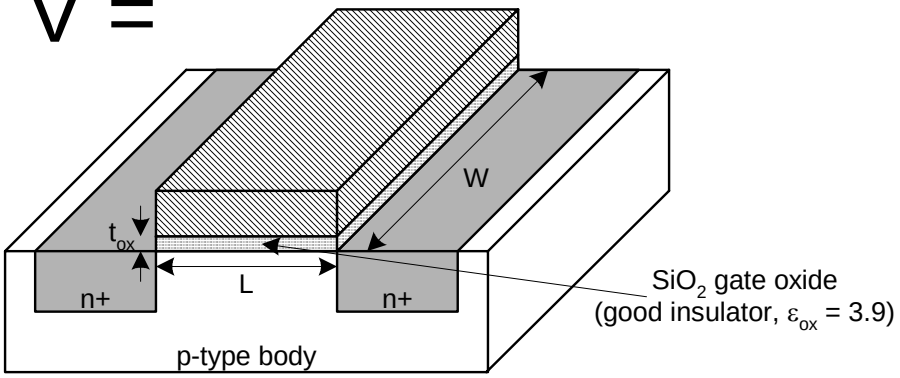
- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel} = CV$
- C =

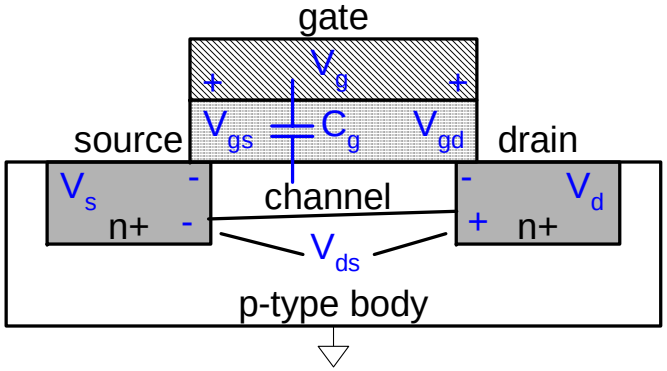




Channel Charge

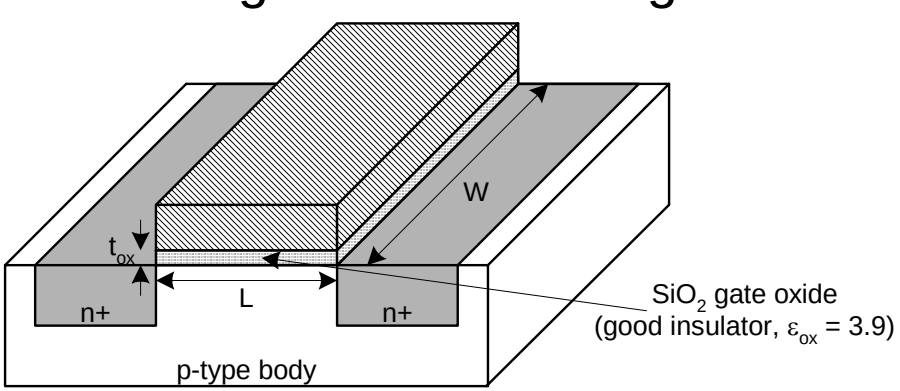
- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL$
- $C_{ox} = \varepsilon_{ox} / t_{ox}$
- V =

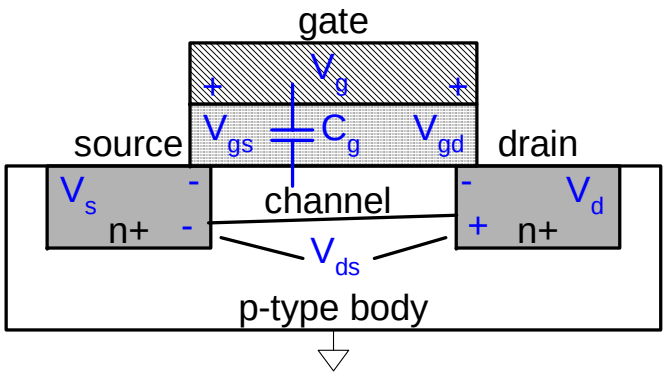




Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{channel} = CV$ $\quad C_{ox} = \varepsilon_{ox} / t_{ox}$
- $C = C_g = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$





Carrier velocity

- Charge is carried by e-
- Carrier velocity *v* proportional to lateral E-field between source and drain
- *v* =

Carrier Velocity

- Charge is carried by e-
- Carrier velocity *v* proportional to lateral E-field between source and drain
- $v = \mu E$ μ called mobility
- E =

Carrier Velocity

- Charge is carried by e-
- Carrier velocity *v* proportional to lateral E-field between source and drain
- $v = \mu E$ μ called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t =$

Carrier Velocity

- Charge is carried by e-
- Carrier velocity *v* proportional to lateral E-field between source and drain
- $v = \mu E$ μ called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t = L / v$

*n*MOS Linear *I-V*

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$I_{ds} =$

*n*MOS Linear *I-V*

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$=$$

*n*MOS Linear *I-V*

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$= \mu C_{\text{ox}} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

$$= \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

$$\beta = \mu C_{\text{ox}} \frac{W}{L}$$

*n*MOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} =$$

*n*MOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta\left(V_{gs} - V_t - V_{dsat}/2\right)V_{dsat}$$

*n*MOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta\left(V_{gs} - V_t - V_{dsat}/2\right)V_{dsat}$$

$$= \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

*n*MOS I-V Summary

- *Shockley* transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

Note the dependencies on W, L

$$\beta = K\frac{W}{L}, K = \frac{C_g \mu}{WL}, C_g = \frac{\in_{ins} \in_0 WL}{D}$$

Activity

1) If the width of a transistor increases, the current will

increase decrease not change

2) If the length of a transistor increases, the current will

increase **decrease** not change

3) If the supply voltage of a chip increases, the maximum transistor current will

increase decrease not change

4) If the width of a transistor increases, its gate capacitance will

increase decrease not change

5) If the length of a transistor increases, its gate capacitance will

increase decrease not change

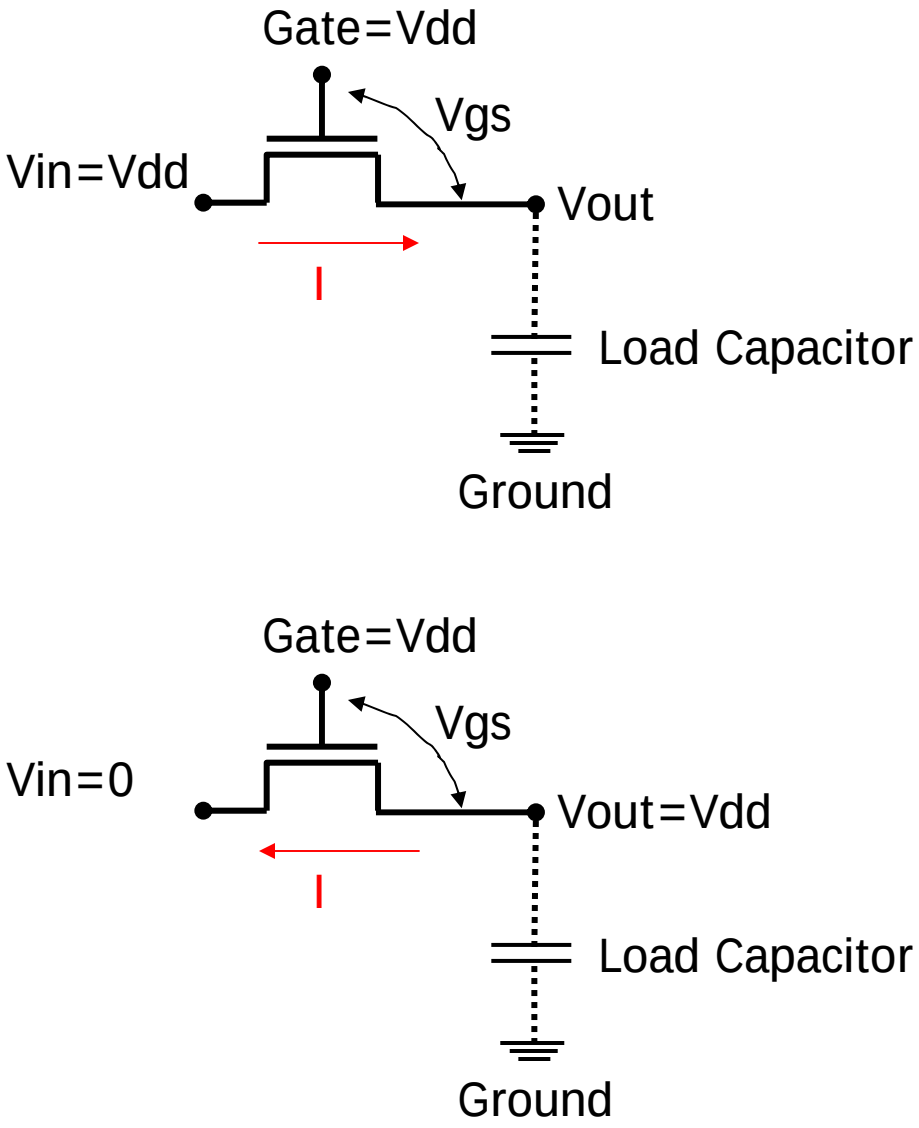
6) If the supply voltage of a chip increases, the gate capacitance of each transistor will

increase decrease **not change**

MOS as switch

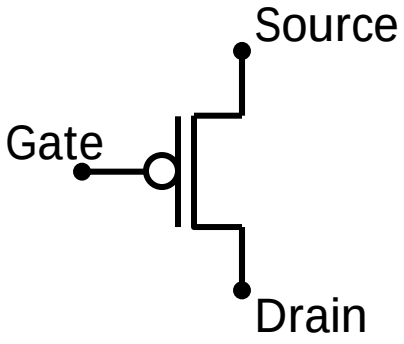
- MOS can be viewed as switches.
- The switches are electrically controlled.

NMOS as a switch



- Assume capacitor (C_L) is initially discharged
- Gate=1, Vin=1
  - C_L begins to conduct and charges toward 1 (Vdd) and stops at (Vdd-Vt)
  - Signal is degraded
- Gate=1, Vin=0
  - C_L begins to discharge toward 0
  - Good passer of 0.

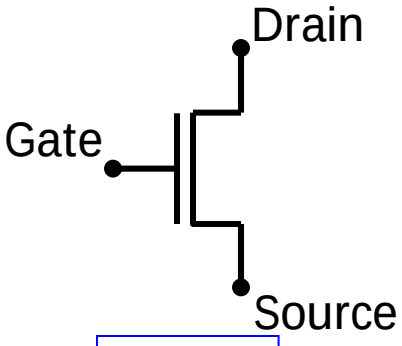
CMOS Signal Transfer Property



pMOS

Gate	Path
0	Closed
1	Open

- Transmits 1 well
- Transmits 0 poorly



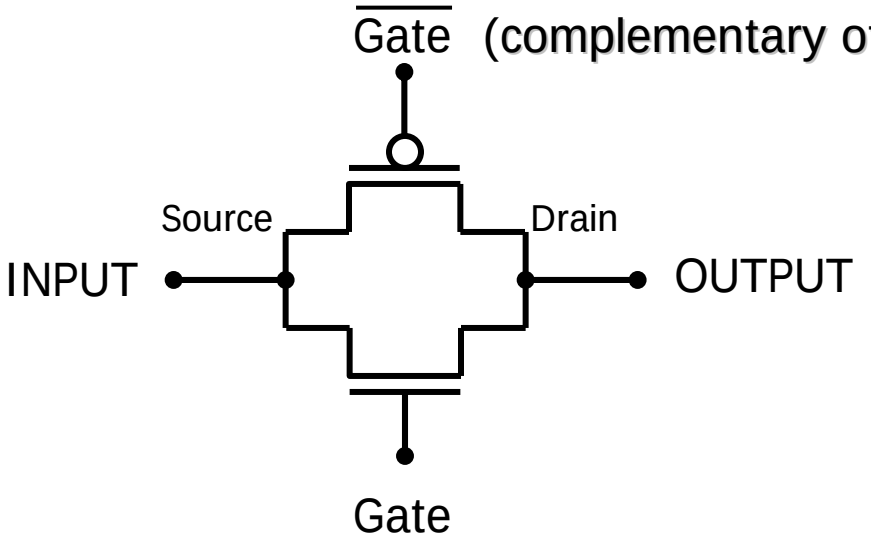
nMOS

Gate	Path
0	Open
1	Closed

- Transmits 0 well
- Transmits 1 poorly

CMOS Transmission Gate

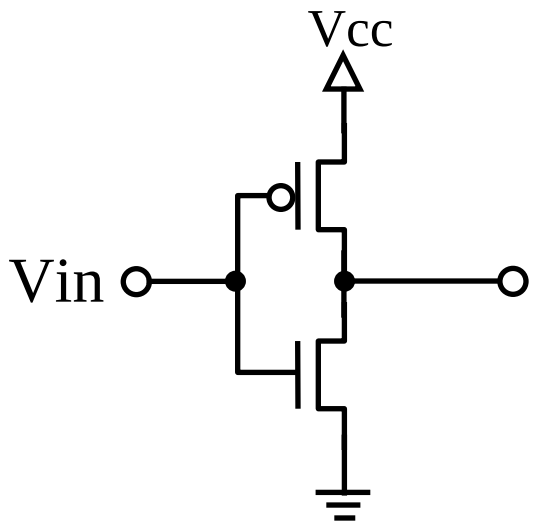
- Transmit signal from INPUT to OUTPUT when Gate is closed



Gate	pMOS	nMOS	OUTPUT
0	OFF	OFF	**Z**
1	ON	ON	INPUT

Z : High-Impedance State,
consider the terminal is “floating”

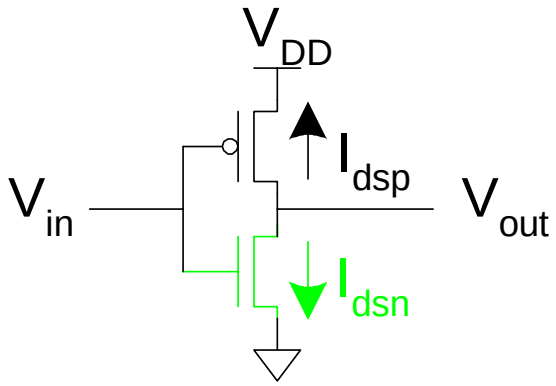
CMOS Inverter



- Combines the best of both.

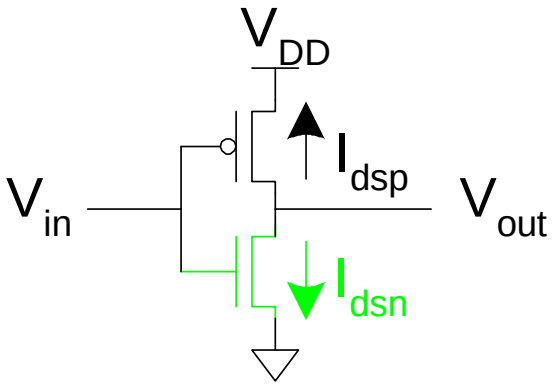
nMOS Operation

Cutoff	**Linear**	**Saturated**
V_{gsn} <	V_{gsn} >	V_{gsn} >
	V_{dsn} <	V_{dsn} >



nMOS Operation

Cutoff	**Linear**	**Saturated**
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$

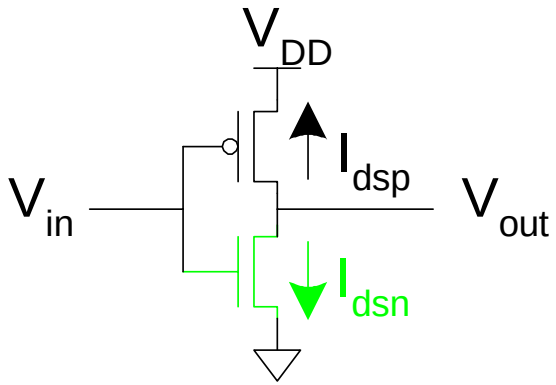


nMOS Operation

Cutoff	**Linear**	**Saturated**
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$

$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$

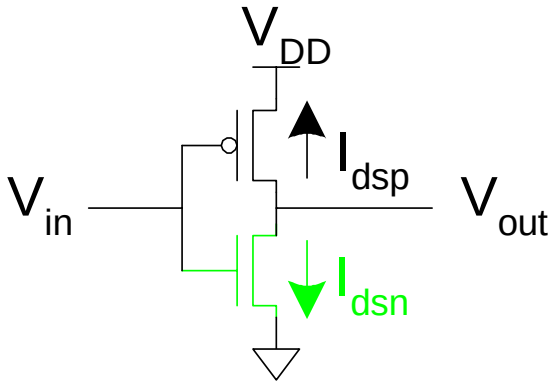


nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} – V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} – V_{tn}$ $V_{out} > V_{in} - V_{tn}$

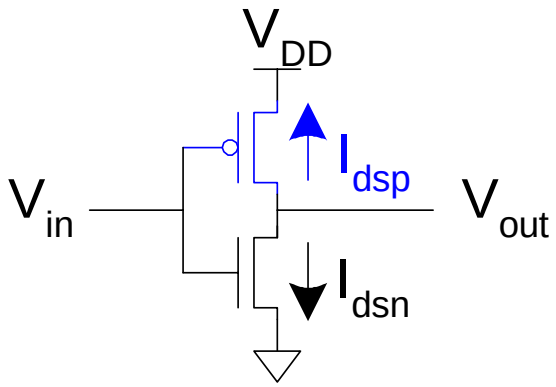
$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$



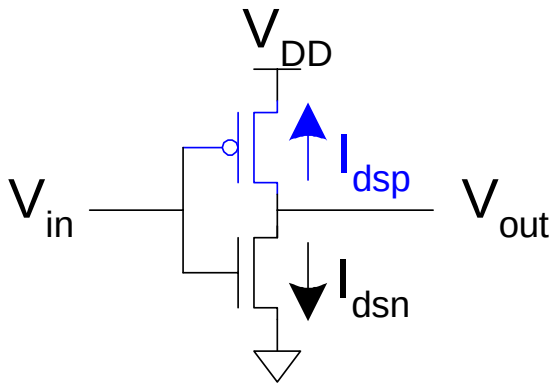
pMOS Operation

Cutoff	Linear	Saturated
V_{gsp} >	V_{gsp} <	V_{gsp} <
	V_{dsp} >	V_{dsp} <



pMOS Operation

Cutoff	**Linear**	**Saturated**
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$



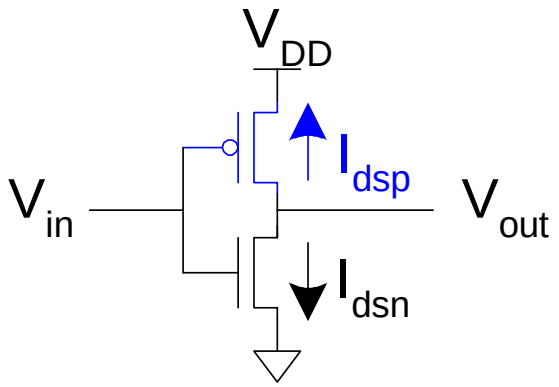
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$

$V_{gsp} = V_{in} - V_{DD}$

$V_{dsp} = V_{out} - V_{DD}$

$V_{tp} < 0$



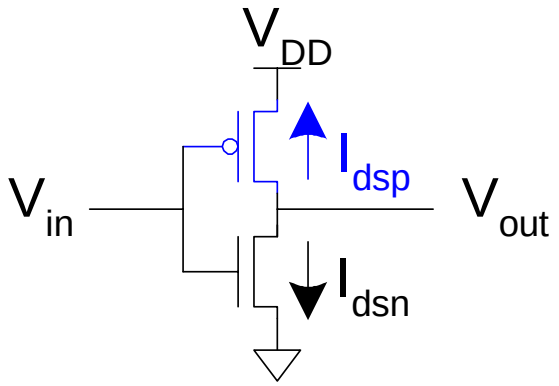
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$ $V_{in} > V_{DD} + V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

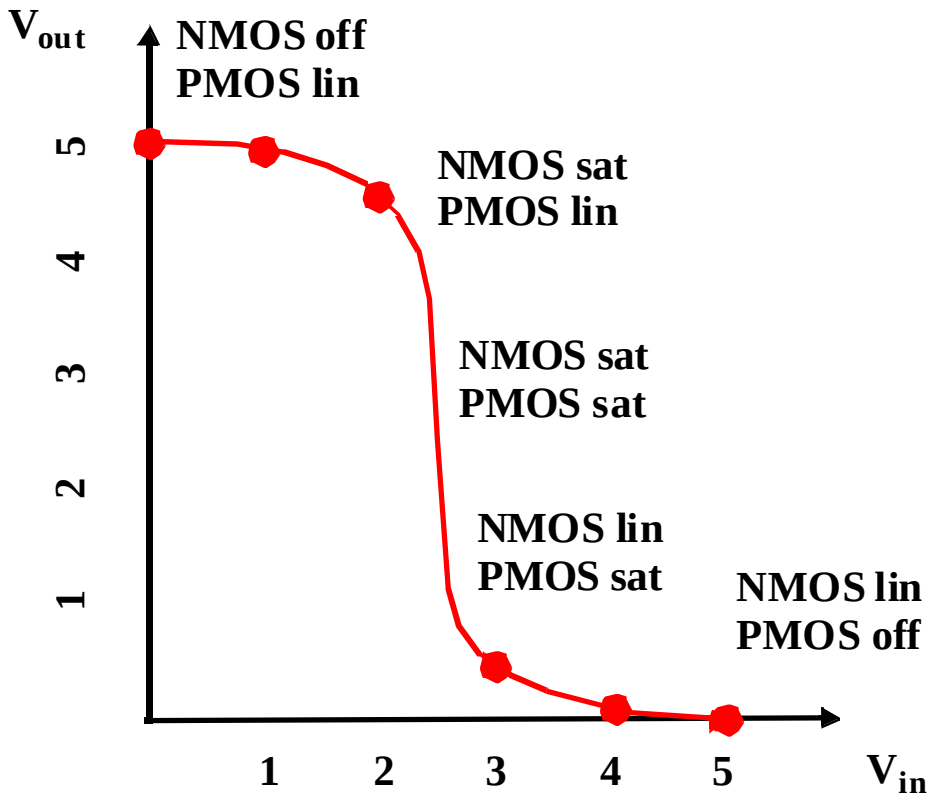
$V_{gsp} = V_{in} - V_{DD}$

$V_{dsp} = V_{out} - V_{DD}$

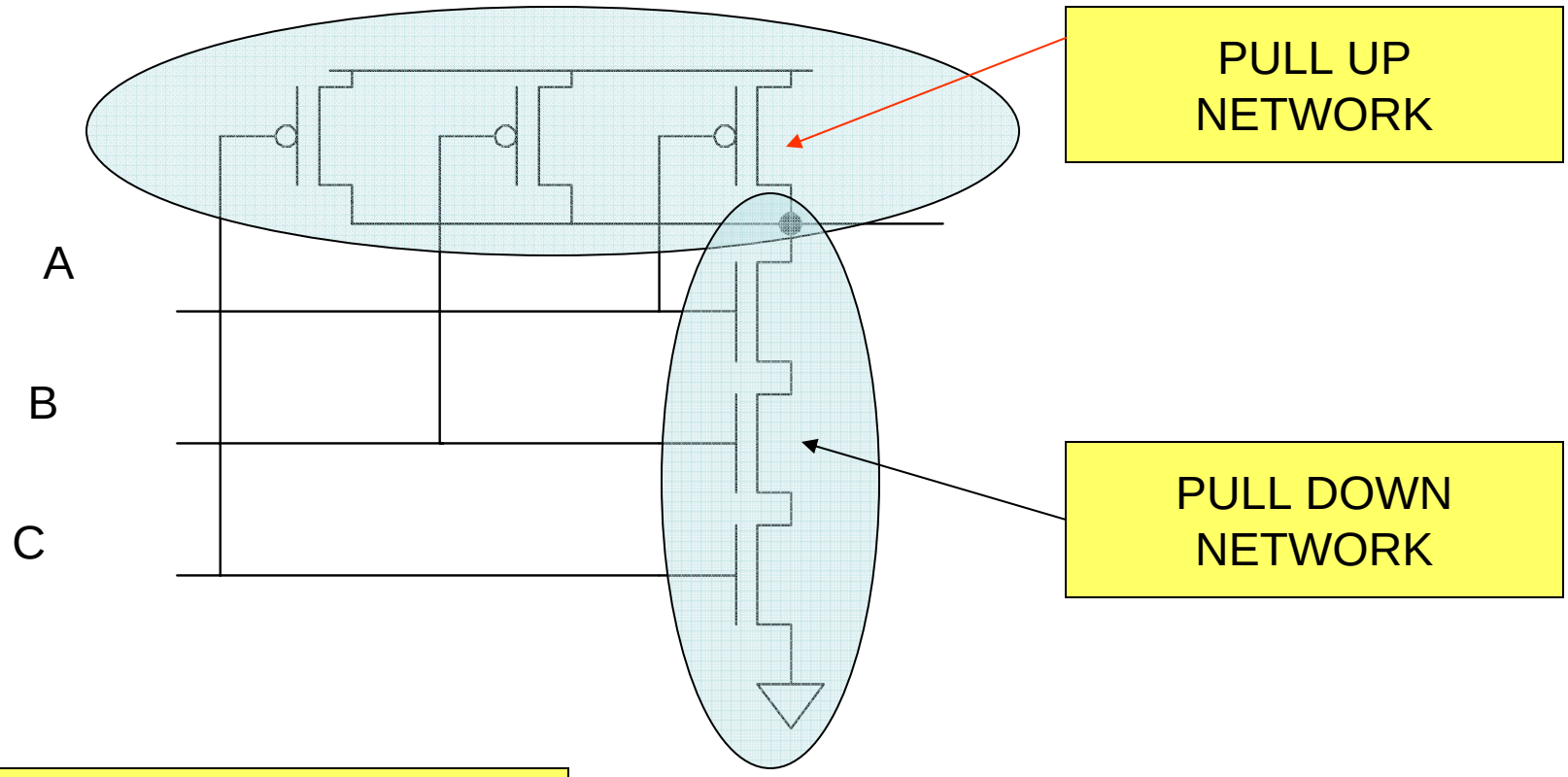
$V_{tp} < 0$



CMOS Inverter Voltage Transfer Characteristic



3 INPUT CMOS NAND GATE



Y=~ABC

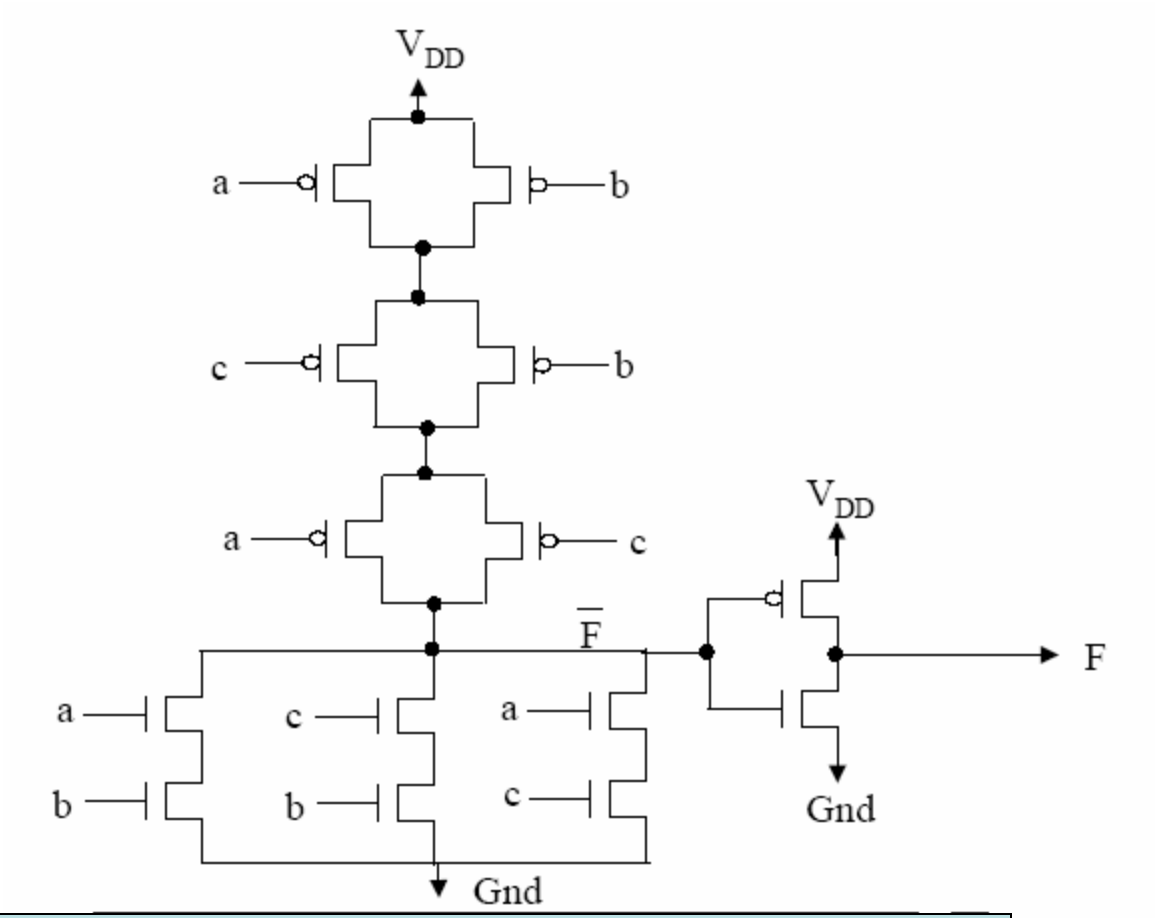
Key Points

- There is always a path from VDD or GND to the output.
- There is no path from the VDD to GND (for our purpose). Thus this gate has a very low power consumption.
- Fully restored logic (why?)

Complex CMOS gates

- Design

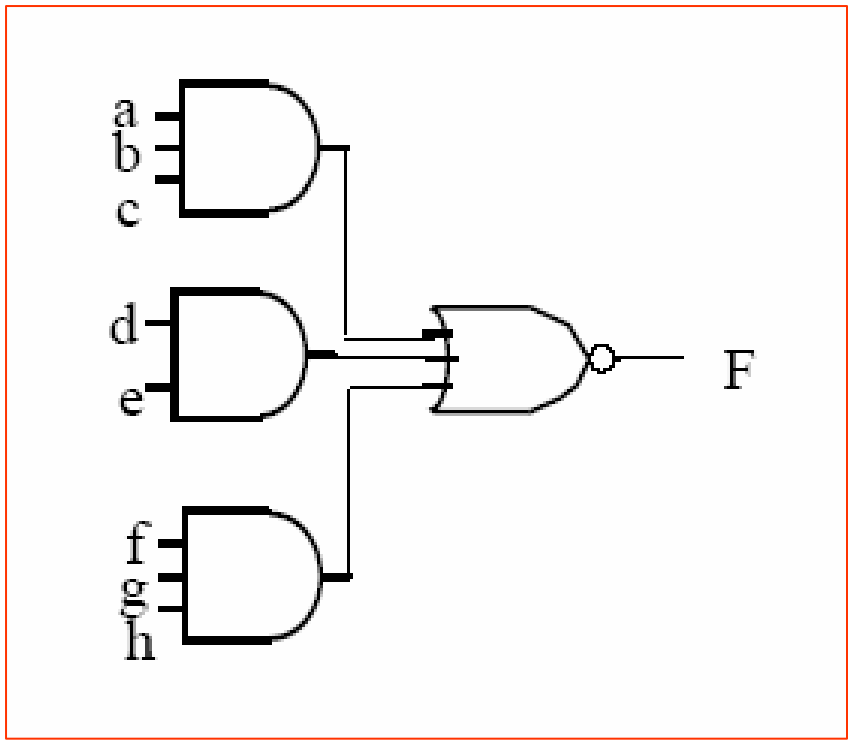
  F=ab+bc+ac



Design the complementary logic…

Exercises

- Design an AND OR Inverter gate:



Tristate Inverter

EN	Inp	Out
0	0	Z
0	1	Z
1	0	1
1	1	0

What will be the CMOS level circuit for the above?

Tristate Inverter

