CAD for VLSI

Project Work

Dt: 25.2.08
Due Date: 31.3.08
Marks 30

Design a 32 bit pipe-lined Wallace Tree **unsigned** multiplier on an FPGA platform. Estimate the following parameters of your design:

1. Resource Utilization (Area)
2. Critical Delay
3. Operating Frequency at post route level
4. Power consumption of the design
5. Compute the area delay product of the design

Ensure that your design is a scalable one. In order to complete your study, plot the area delay product, area and delay wrt the bit size of the multiplier. Comment on the scalability of the Wallace Tree multiplier wrt an array multiplier based on your observation.

Note: Extra credit shall be awarded for taking care in optimizing the critical path delay and the area required.