INDIAN INSTITUTE OF TECHNOLOGY
KHARAGPUR

Signature of the Invigilator

Please fill up carefully the boxes provided below

EXAMINATION (Mid Semester)	SEMESTER (Spring)

Roll Number									Section		Name	
Subject Number	C	S	2	1	0	0	2	Subject Name	Switching Circuits and Logic Design			
Name of the Department / Center of the Student												

Instructions and Guidelines to Students Appearing in the Examination

1. Ensure that you have occupied the seat as per the examination schedule.
2. Ensure that you do not have a mobile phone or a similar gadget with you even in switched off mode. Note that loose papers, notes, books should not be in your possession, even if those are irrelevant to the paper you are writing.
3. Data book, codes or any other materials are allowed only under the instruction of the paper-setter.
4. Use of instrument box, pencil box and non-programmable calculator is allowed during the examination. However, exchange of these items is not permitted.
5. Additional sheets, graph papers and relevant tables will be provided on request.
6. Write on both sides of the answer script and do not tear off any page. Report to the invigilator if the answer script has torn page(s).
7. Show the identity card whenever asked for by the invigilator. It is your responsibility to ensure that your attendance is recorded by the invigilator.
8. You may leave the examination hall for wash room or for drinking water, but not before one hour after the commencement of the examination. Record your absence from the examination hall in the register provided. Smoking and consumption of any kind of beverages is not allowed inside the examination hall.
9. After the completion of the examination, do not leave the seat until the invigilator collects the answer script.
10. During the examination, either inside the examination hall or outside the examination hall, gathering information from any kind of sources or any such attempts, exchange or helping in exchange of information with others or any such attempts will be treated as adopting 'unfair means'. Do not adopt 'unfair means' and do not indulge in unseemly behavior as well.

Violation of any of the instructions may lead to disciplinary action of varied nature.

To be filled in by the examiner

Question	1	2	3	4	5	6	7	8	9	10	**Total** / **95**
Marks obtained											

Total marks obtained (in words)	Signature of Examiner	Signature of Scrutineer

Wed, Feb 19, 2020, 9-11am	Students: 145	Venue: F116, F142, NR113, NR114, NR412

Answer ALL the questions.
Do all rough work on on the blank page included in the questions paper.
Answer on the question paper itself in the spaces provided.
There may be more blank spaces than what are minimally needed to answer the questions.

1. Simplify the following functions

   (a) $f(a,b,c,d) = \prod_M(3,6,8,9,10)$[off-set] $\cdot \prod_D(0,1,2,7)$[don't care set] for 2-level product-of-sum (POS) realisation (negated literals permitted). 10

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a,b \ c,d	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

Consider the following sums:

$d_1 = \sum(2,3,7,6) = (a+\bar{c})$,

$d_2 = \sum(0,1,8,9) = (b+c)$,

$d_3 = \sum(0,2,8,10) = (b+d)$,

$f(a,b,c,d) = d_1 \cdot d_2 \cdot d_3$

(b) $f(a,b,c,d,e) = \sum_m(0,4,6,7,8,12,14,16,18,19,20,24,26,28)$ [on-set] $+ \sum_D(2,3,10,15,22,23,27,30)$ [don't care set] for 2-level realisation using XOR and AND gates (negated literals permitted). 15

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a,b \ c,d,e	000	001	011	010	110	111	101	100
00	0	1	3	2	6	7	5	4
01	8	9	11	10	14	15	13	12
11	24	25	27	26	30	31	29	28
10	16	17	19	18	22	23	21	20

Consider the following cubes:

$c_1 = \prod(0,4,8,12,16,20,24,28) = \bar{d}\bar{e}$,

$c_2 = \prod(2,3,6,7,10,11,14,15) = \bar{a}\bar{d}$,

$c_2 = \prod(2,3,10,11,18,19,26,27) = \bar{c}d$,

Thus, $f(a,b,c,d,e) = c_1 \oplus c_2 \oplus c_3$

2. Let $X_n = \langle x_{n-1} \ldots x_1 x_0 \rangle$ and $Y_n = \langle y_{n-1} \ldots y_1 y_0 \rangle$ be two unsigned numbers of n bits with the rightmost bit as the LSB. Let the LT-comparison of X and Y be defined as: $f_n(X_n, Y_n) = \begin{cases} 1 & \text{if } X < Y \\ 0 & \text{otherwise} \end{cases}$

(a) Present a recursive definition of $f_n(X_n, Y_n)$ suitable for realisation using a network of gates. 5

$f_1(\langle x_0 \rangle, \langle y_0 \rangle) = \bar{x}_0 y_0$

$f_n(\langle x_{n-1} \ldots x_1 x_0 \rangle, \langle y_{n-1} \ldots y_1 y_0 \rangle) =$

$\bar{x}_{n-1} y_{n-1} + \overline{x_{n-1} \bar{y}_{n-1}} f_{n-1}(\langle x_{n-2} \ldots x_1 x_0 \rangle, \langle y_{n-2} \ldots y_1 y_0 \rangle)$

$\bar{x}_{n-1} y_{n-1} + (\bar{x}_{n-1} + y_{n-1}) f_{n-1}(\langle x_{n-2} \ldots x_1 x_0 \rangle, \langle y_{n-2} \ldots y_1 y_0 \rangle)$

(b) Based on the above recursive definition, design a circuit block for realising the LT-comparison of two bits (i.e. $f_1(X_1, Y_1)$) and other required (sub-)functions, so that it may be used to achieve LT-comparison of m bits; let this block be S. 5

$l_i = \bar{x}_i y_i$

$d_i = \bar{x}_i + y_i$

Gate network corresponding to above expressions

(c) Using the S circuit blocks, present a simple circuit to realise $f_n(X_n, Y_n)$, for arbitrary n, (additional glue logic may be used, as required, assume that k-input gates for $k \leq 6$ are available). 10

Rippling comparator according to the expressions for 2b

(d) Let the delay of a gate (AND/OR/NAND/NOR) be Δ; derive the delay of the circuit designed above (in part 2c) to compute $f_n(X_n, Y_n)$ (disregard the cost accrued due to negated literals). 5

$\mathcal{O}(n)$

(e) Using the outputs of S, develop a lookahead circuit block B_m (of constant delay) which may be used to compute $f_m(X_m, Y_m)$ for m-bit words. Later, B_m is to be used to compute $f_n(X_n, Y_n)$ (assume n is a multiple of m) with a delay of $\mathcal{O}(\lg_m n)$ (assume that AND/OR/NAND/NOR gates with $\mathcal{O}(m)$ inputs are available, i.e. m is relatively small). 10

$L_m = l_{m-1} + d_{m-1}l_{m-2} + d_{m-1}d_{m-2}l_{m-3} + \ldots + d_{m-1}d_{m-2}\cdots d_1 d_0 L_{\text{in}}$

$L_{\text{out}} = l_{m-1} + d_{m-1}l_{m-2} + d_{m-1}d_{m-2}l_{m-3} + \ldots + d_{m-1}d_{m-2}\cdots d_1 l_0$

$D_{\text{out}} = d_{m-1}d_{m-2}\cdots d_1 d_0$

Same circuit structure as BCLA unit for 4 bits, taking $m = 4$

(f) What will the cost of this scheme, B_m for $m = 4$ in the number of gates (disregard the cost accrued due to negated literals)? 5

cost $= 14+9+5+2+9+3 = 42$, according to the terms below

$L_3 = l_3 + d_3 l_2 + d_3 d_2 l_1 + d_3 d_2 d_1 l_0 + d_3 d_2 d_1 d_0 L_{\text{in}}$

$L_2 = l_2 + d_2 l_1 + d_2 d_1 l_0 + d_2 d_1 d_0 L_{\text{in}}$; $L_1 = l_1 + d_1 l_0 + d_1 d_0 L_{\text{in}}$; $L_0 = l_0 + d_0 L_{\text{in}}$

$L_{\text{out}} = l_3 + d_3 l_2 + d_3 d_2 l_1 + d_3 d_2 d_1 l_0$

$D_{\text{out}} = d_3 d_2 d_1 d_0$

(g) Using the scheme B_m for m-bit words, present a circuit for computing f_{m^2} efficiently (so that the circuit has constant $\left(\propto \lg_m m^2\right)$ delay assuming that AND/OR/NAND/NOR gates with $\mathcal{O}(m)$ inputs are available, i.e. m is relatively small); you may instantiate the design for $m = 4$. 5

Same circuit structure as BCLA for 16 bits, taking $m = 4$

3. Prove the following (for Boolean operators, variables and functions):

(a) $xa + \bar{x}b = xa + \bar{x}b + ab$ [Prove algebraically]. 5

$xa + \bar{x}b + ab = xa + \bar{x}b + (x + \bar{x})ab = xa(1 + b) + \bar{x}b(1 + a) = xa + \bar{x}b$

(b) $f(x_1, x_2, \ldots, x_n) = x_1 f(1, x_2, \ldots, x_n) + \bar{x}_1 f(0, x_2, \ldots, x_n)$. 5

By perfect induction:

Let $x_1 = 0$

LHS: $f(0, x_2, \ldots, x_n)$

RHS: $0 \cdot f(1, x_2, \ldots, x_n) + 1 \cdot f(0, x_2, \ldots, x_n) = f(0, x_2, \ldots, x_n)$

Let $x_1 = 1$

LHS: $f(1, x_2, \ldots, x_n)$

RHS: $1 \cdot f(1, x_2, \ldots, x_n) + 0 \cdot f(0, x_2, \ldots, x_n) = f(1, x_2, \ldots, x_n)$

4. Simplify $f(w,x,y,z) = \sum_m (2,6,8,9,10,11,14,15)$ using the QM method

Final solution: 6

$f = w\bar{x} + wy + y\bar{z}$

Present the working below: 9

2 no of 1's	
m	**w x y z**
6	0 1 1 0
9	1 0 0 1
10	1 0 1 0

3 no of 1's	
m	**w x y z**
11	1 0 1 1
14	1 1 1 0

(2, 1)	
Cube	**w x y z**
6, 14	- 1 1 0
9, 11	1 0 - 1
10, 11	1 0 1 -
10, 14	1 - 1 0

3 no of 1's	
m	**w x y z**
11	1 0 1 1
14	1 1 1 0

4 no of 1's	
m	**w x y z**
15	1 1 1 1

(3, 1)	
Cube	**w x y z**
11, 15	1 - 1 1
14, 15	1 1 1 -

(1, 1)	
Cube	**w x y z**
2, 6	0 - 1 0
2, 10	- 0 1 0
8, 9	1 0 0 -
8, 10	1 0 - 0

(2, 1)	
Cube	**w x y z**
6, 14	- 1 1 0
9, 11	1 0 - 1
10, 11	1 0 1 -
10, 14	1 - 1 0

(1, 2)	
Cube	**w x y z**
2, 6, 10, 14	- - 1 0
8, 9, 10, 11	1 0 - -

(2, 1)	
Cube	**w x y z**
6, 14	- 1 1 0
9, 11	1 0 - 1
10, 11	1 0 1 -
10, 14	1 - 1 0

(3, 1)	
Cube	**w x y z**
11, 15	1 - 1 1
14, 15	1 1 1 -

(2, 2)	
Cube	**w x y z**
10, 11, 14, 15	1 - 1 -

Prime Implicants	2	6	8	9	10	11	14	15
2, 6, 10, 14	ⓧ	ⓧ			X		X	
8, 9, 10, 11			ⓧ	ⓧ	X	X		
10, 11, 14, 15					X	X	X	ⓧ

$f = wy + w\bar{x} + y\bar{z}$