INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

Computer Science and Engineering

Switching Circuits and Logic Design (CS21002)

Class Test – I (Spring)

Name: ______________________ *Roll number:* ______________

Date: Wed, Feb 05, 2020 *Marks:* 90 *Time:* 6:15-7:15pm (AN)

Place: CSE-107, CSE-108, CSE-119, CSE-120, CSE-302 *Students:* 72+73=145

Answer ALL the questions.
Do rough work on available blank pages/sheets.

Q1: Run the *double dabble* (also called *add-3 and shift*) algorithm to convert the binary number 110100101 to BCD showing each step clearly. The operations should be either `L Sft` for left shift or `Add 3`. The entries for B1, B2 and B3 should be their values after application of the indicated operation. 50

Operation	B2	B1	B0	421
Start	0000	0000	0000	110100101
L Sft	0000	0000	0001	110100101
L Sft	0000	0000	0011	110100101
L Sft	0000	0000	0110	110100101
Add 3	0000	0000	1001	110100101
L Sft	0000	0001	0011	110100101
L Sft	0000	0010	0110	110100101
Add 3	0000	0010	1001	110100101
L Sft	0000	0101	0010	110100101
Add 3	0000	1000	0010	110100101
L Sft	0001	0000	0101	110100101
Add 3	0001	0000	1000	110100101
L Sft	0010	0001	0000	110100101
L Sft	0100	0010	0001	110100101
Finish	4	2	1	

Q2: Represent 29 and -17 in 8-bit signed 2's complement representation; then perform the following operations on your representations, showing each step clearly:

(a) 29+(-17) 10

Item	Binary representation
17	0001 0001
-17 (2's complement)	1110 1111
29	0001 1101
+ (-17)	1110 1111
Result 12	0000 1100

(b) (-17)+(-29) 10

Item	Binary representation
29	0001 1101
-29 (2's complement)	1110 0011
-17	1110 1111
+ (-29)	1110 0011
Result -46	1101 0010

Q3: Bits 1111011 corresponding to $\langle p_1, p_2, d_1, p_3, d_2, d_3, d_4 \rangle$ for single bit ECC Hamming code is received; here d_1, d_2, d_3 and d_4 are the data bits while p_1, p_2 and p_3 are the parity bits. Assume that at most one of the bits that are received may be corrupted (i.e. $\bar{b}$ received instead of b). 20

Association of parity bits to the data bits may be done according to the table below.

Bits positions (starting at 1)	7	6	5	4	3	2	1
Binary	111	110	101	100	011	010	001
Received data/parity bit	d_4	d_3	d_2	p_3	d_1	p_2	p_1
Association	p_3, p_2, p_1	p_3, p_2	p_3, p_1	p_3	p_2, p_1	p_2	p_1
Recomputed bit name	d_4^r	d_3^r	d_2^r	p_3^r	d_1^r	p_2^r	p_1^r

Let e_i be the Boolean value that is 1 if and only if the parity condition involving bit p_i is violated. Fill up the following table to present the Boolean expression (using $\cdot, +, \oplus, \leftrightarrow, '$) for e_i in terms of the received bits.

Parity violation indicator	Boolean expression to compute parity violation	Truth value
e_1	$e_1 =$ $p_1 \oplus d_1 \oplus d_2 \oplus d_4$	1
e_2	$e_2 =$ $p_2 \oplus d_1 \oplus d_3 \oplus d_4$	0
e_3	$e_3 =$ $p_3 \oplus d_2 \oplus d_3 \oplus d_4$	1

Fill up the following table to present the Boolean expression (using $\cdot, +, \oplus, \leftrightarrow, '$) to capture that an error has occured in the indicated bit, as error flags (EF); your expressions should be in terms of e_1, e_2, e_3.

Bit	Value	EF	Boolean expression to compute error flag	EF value
p_1	1	f_1	$f_1 =$ $e_1 \cdot e_2' \cdot e_3'$	0
p_2	1	f_2	$f_2 =$ $e_1' \cdot e_2 \cdot e_3'$	0
p_3	1	f_3	$f_3 =$ $e_1' \cdot e_2' \cdot e_3$	0
d_4	1	g_4	$g_4 =$ $e_1 \cdot e_2 \cdot e_3$	0
d_3	1	g_3	$g_3 =$ $e_1' \cdot e_2 \cdot e_3$	0
d_2	0	g_2	$g_2 =$ $e_1 \cdot e_2' \cdot e_3$	1
d_1	1	g_1	$g_1 =$ $e_1 \cdot e_2 \cdot e_3'$	0

Finally, fill up the following table to present the Boolean expression (using $\cdot, +, \oplus, \leftrightarrow, '$) in terms of received bits and the computed flag bits that will allow the correct bits to be recovered.

Recomputed bit	Boolean expression to recompute the bit	Recomputed value
p_1^r	$p_1^r =$ $p_1 \oplus f_1$	1
p_2^r	$p_2^r =$ $p_2 \oplus f_2$	1
p_3^r	$p_3^r =$ $p_3 \oplus f_3$	1
d_4^r	$d_4^r =$ $d_4 \oplus g_4$	1
d_3^r	$d_3^r =$ $d_3 \oplus g_3$	1
d_2^r	$d_2^r =$ $d_2 \oplus g_2$	1
d_1^r	$d_1^r =$ $d_1 \oplus g_1$	1