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Sumana Ghosh

Contact Information

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Research Interests

Design, Verification, and Analysis of Embedded Control Systems, Application of Formal Techniques in Real-Time Scheduling and Fault-tolerant Control Design, Cyber-Physical Systems Security, and Formal Methods.

Education

Doctor of Philosophy(Ph.D.) 2013 – 2019

Dept. of Computer Science and Engg., Indian Institute of Technology (IIT) Kharagpur, India.
Thesis Topic: **Formal Approach towards Pattern Guided Scheduling in Embedded Control Systems**
Area of Study: Embedded Control Systems, Formal Verification
Supervisors: Prof. Pallab Dasgupta and Prof. Soumyajit Dey
Worked At: Formal Verification Research Group, Dept. of Computer Science and Engg., Indian Institute of Technology Kharagpur.

M.Sc in Computer & Information Science 2010 – 2012
University of Calcutta (81%)

B.Sc in Computer Science 2007 – 2010
University of Calcutta (68.88%)

Higher Secondary Examination (Class-12) 2005 – 2007
West Bengal Council of Higher Secondary Education (81.2%)

Secondary Examination (Class-10) 2004 – 2005
West Bengal Board of Secondary Education (82.6%)

Publication

Journals

- Sumana Ghosh, Soumyajit Dey, Pallab Dasgupta; "Pattern Guided Integrated Scheduling and Routing in Multi-hop Control Networks", Accepted for the publication in ACM Transaction on Embedded Computing Systems (TECS) 2020.

- Sumana Ghosh, Soumyajit Dey, Pallab Dasgupta; "Performance and Energy Aware Robust Specification of Control Execution Patterns under Dropped Samples", IET Computers & Digital Techniques (CDT), Volume: 13, Issue: 6, pp: 493–504(11), Nov, 2019, DOI: 10.1049/iet-cdt.2019.0030.

- Sumana Ghosh, Soumyajit Dey, Pallab Dasgupta; "Co-synthesis of Loop Execution Patterns for Multi-Hop Control Networks", IEEE Embedded System Letters (ESL), Volume: 10, Issue 4, pp 111-114, Dec. 2018, DOI: 10.1109/LES.2017.2777506.

- Sumana Ghosh, Souradeep Dutta, Soumyajit Dey, Pallab Dasgupta; "A Structured Methodology for Pattern based Adaptive Scheduling in Embedded Control ", ACM Transactions on Embedded Computing Systems, part of the ESWEEK-TECS special issue, presented in the International Conference on Embedded Software, Volume:16, No: 5s, Article:189, Sept. 2017, DOI : 10.1145/3126514.

Conferences

- Sumana Ghosh, Soumyajit Dey, Pallab Dasgupta; "Synthesizing Performance-aware (m,k)-firm Control Execution Patterns under Dropped Samples", In the International Conference on VLSI Design (VLSID), pages 1-6, Jan. 2019, DOI:10.1109/VLSID.2019.00019. **Best Paper Award Nominee and won Honorable Mention Award.**

- Sumana Ghosh, Souradeep Dutta, Soumyajit Dey, Pallab Dasgupta; "A Structured Methodology for Pattern based Adaptive Scheduling in Embedded Control ", In the International Conference on Embedded Software (EMSOFT), journal version appeared in ACM TECS, Seoul, South Korea, Sept. 2017, DOI : 10.1145/3126514.

- Sumana Ghosh, Pallab Dasgupta; "Formal Methods for Pattern Based Reliability Analysis in Embedded Systems", In the International Conference on VLSI Design (VLSID), pages 192-197, Jan. 2015, DOI: 10.1109/VLSID.2015.38.

Journals Under Review

- Sumana Ghosh, Soumyajit Dey, Pallab Dasgupta; "Performance driven Post Processing of Control Loop Execution Schedules", Communicated in ACM Transaction on Design Automation of Electronic Systems (TODAES).

Research Experience

Ph.D. Research, Indian Institute of Technology Kharagpur

Title: *Formal Approach towards Pattern Guided Scheduling in Embedded Control Systems*

Abstract: The growing demand for mapping diverse embedded applications on shared processors has brought focus on control-scheduling co-design approaches. These co-design approaches address the joint optimization of control parameters (such as control performance) and scheduling parameters (such as resource utilization) while guaranteeing the timing properties of all software tasks, combining the knowledge of feedback control theory and real-time scheduling theory. In the co-design context, to cope with multiple design trade-offs between control and platform parameters, aperiodic execution of controllers has become a promising alternative to the traditional periodic executions. This research work primarily focuses on such aperiodic pattern guided execution of the controllers and proposes with a bouquet of new formalisms and frameworks for efficiently addressing various aspects of this control-scheduling co-design problem. This research develops an adaptive scheduling framework for a set of control loops by introducing the notion of loop execution patterns. A structured synthesis mechanism is proposed for generating such loop execution patterns under different input disturbance scenarios. The proposed synthesis methodology employs stable adaptive switching between loop execution patterns for improved quality of control and resource utilization while guaranteeing the schedulability of the loops. This research presents a unique framework for post-processing a static schedule of a set of control loops such that combined control performance can be improved further. The proposed method instruments each loop to switch between multiple controllers by co-operatively sharing their execution slots. This research provides a fault tolerant framework for synthesizing the specifications of a set of loop execution patterns, that are robust enough to guarantee the desired control performance under platform non-idealities. The synthesis process is developed leveraging the concept of bounded model checking for generating such robust specifications. This research develops a co-design framework to synthesize a co-schedulable combination of loop execution patterns for a set of control loops over a shared wireless multi-hop control network, along with their associated routing solution, such that overall control performance gets optimized. The proposed framework is also shown to be useful for evaluating the fault tolerance of a resource-constrained shared network subject to communication link failures.

Current Ongoing Research Activities, Indian Institute of Technology Kharagpur

Currently, I am working in two other research projects with other group members of the Formal Methods Lab at IIT Kharagpur. One of these research works focuses on the development of an affordable cyber-physical system testbed useful for performance evaluation of associated control and scheduling algorithms against various faults like packet drops, transmission errors, fault attacks, etc. Other research work aims to develop a pattern guided provably stable as well as secure scheduling schemes for embedded control against false data injection attacks.

Professional Experience

Sponsored Research and Industrial Consultancy (SRIC), IIT Kharagpur

- FMSAFE: A Networked Centre for Formal Methods in Validation and Certification Procedures for Safety Critical ICT Systems.
  - My Working Period: January 2018 - January 2019.
  - Sponsored by: MHRD and Ministry of Railways.
  - Partners: IIT Kharagpur, IIT Kanpur, IIT Bombay.
  - In this project IIT Kharagpur team's activity is to develop an SMT-based tool for modeling and validation of hybrid dynamical systems comprising software, platform and plant.

- AUTOSAFE: Architecture-aware Timing Analysis and Optimization of Safety-Critical Automotive Software.
  - My Working Period: July 2014 - December 2015.
  - Sponsored by: Indo-German Science and Technology Center (IGSTC).
  - Partners: IIT Kharagpur, Technical University Munich (TUM), Germany, Tata Research Development and Design Center (TRDDC), India, INCHRON GmbH, Germany.
  - In this project a tool, AUTOSAFE, has been developed which does an architecture-aware timing analysis of an automotive software.

Academic Activities

- Organized a two-day Indo-Israel joint research workshop between IIT Kharagpur and Ben-Gurion University, Israel, held at IIT Kharagpur, February 2016.
- Organized a one-day Indo-German technical workshop "*AUTOSAFE: Design of High Assurance Automotive Control*", held at IIT Kharagpur, December 2015.
- Local Organizing Committee Member of *Formal Methods Update Meeting*, India, 2014.
- Reviewer for various conferences and journals; VLSI Design 2015, 2017, 2018, Euromicro Conference on Digital System Design 2018, 2019, IET-CDT 2019.

Talks Delivered

- Presented "*Synthesizing Performance-aware (m,k)-firm Control Execution Patterns under Dropped Samples*", at the IEEE VLSID Conference, January 2019, held at New Delhi, India.
- Presented "*A Structured Methodology for Pattern based Adaptive Scheduling in Embedded Control*", at the ACM SIGBED International Conference on Embedded Software (EMSOFT), October 2017, held at Seoul, South Korea.
- Presented "*Formal Methods for Pattern Based Reliability Analysis in Embedded Systems*", at the IEEE VLSID Conference, January 2015, held at Bangalore, India.
- Delivered talk on "*Formal Methods for Verification of Real-Time Embedded Control* ", at the Indo-Israel Workshop, February 2016, held at IIT Kharagpur.
- Delivered talk on "*An Algorithmic Bridge from Adaptive Sampling to Automata-based Scheduling for Embedded Control*", at the Indo-German Workshop, December 2015, held at IIT Kharagpur.

Honors and Awards

- Received Honorable Mention Award in VLSID Conference 2019.
- Received Microsoft Research travel grant and ACM-India IARCS grant for attending ACM-SIGBED EMSOFT Conference 2017, Seoul, South Korea.
- Awarded Scholarship for attending the international conference CAV 2016 and VMW workshop 2016, Toronto, Ontario, Canada.
- Awarded Research Fellowship by Ministry of Human Resource Development (MHRD) for a tenure of 5 years (2013 - 2018).

- Qualified UGC NET (University Grants Commission - National Eligibility Test) with *Junior Research Fellowship* award in Computer Science and Application, December 2012.
- The prestigious *Mamraj Agarwal National Award* and *University Gold Medal* for standing First in M.Sc Exam, 2012.
- M.Sc (Computer and Information Science), *First Class First*, University of Calcutta, 2012.
- Qualified GATE (Graduate Aptitude Test in Engineering) in Computer Science and Information Technology in 2012 with a score of 652.

Member of Professional Bodies

Student Member, IEEE India
Women in Engineering, IEEE India

Computing Skills

Programming and Scripting Languages: C, C++, Python, JAVA, MATLAB-Simulink, Perl, SQL, HTML, PHP, Shell Scripting, Prolog, Verilog, Microprossor 8085 programming.

Tools :
- Model Checker Tools: NuSMV (Carnegie Mellon University), Magellan (Synopsys), PRISM (University of Birmingham and the University of Oxford), UPPAAL (Uppsala University and Aalborg University), ABC (University of California, Berkeley).
- SAT Solver Tools: Zchaff (Princeton University), Z3-SMT Solver (Microsoft Research).
- ILP Solver Tool: CPLEX (IBM)

Teaching and Mentoring Experience

As Teaching Assistant: Performed the role of teaching assistant for the following courses during Ph.D. Teaching assistants in IIT Kharagpur are entrusted with many duties which differ from course to course and primarily include delivering occasional lectures, preparing tutorials, assignments, and class-test questions, evaluating and grading class-test answer scripts and assignments, (in)formal interactions with the students, serving as invigilators, etc.
- Formal Languages & Automata Theory (CS21004; Assisted thrice: Spring 2018, 2017, 2014; Level: UG)
- Computational Foundation of Cyber-physical Systems (CS61063; Assisted twice: Autumn 2017, 2018; Level: PG)
- Programming & Data Structures Lab (CS19001; Assisted thrice: Autumn 2016, 2015, Spring 2013; Level: UG)
- Database Management Systems (CS43002; Assisted twice: Spring 2016, 2015; Level: UG)
- Advance Graph Theory (CS60047; Assisted once: Autumn 2014; Level: PG)
- Foundations of Computing Science (CS60001; Assisted once: Autumn 2013; Level: PG)

As Teaching Assistant: Performed the role of teaching assistant in a programme named "Train 10,000 Teachers (T10kT)", under the project 'Empowerment of Students/Teachers', sponsored by National Mission on Education through ICT (MHRD, Government of India), 2015. I specially assisted the course *Introduction to Algorithm Design* in two workshops under this programme. In first phase, 300 teachers form different engineering colleges in India, came IIT Khragpur to attend the 1-week workshop, where they were taught by three prominent faculties of CSE department of IIT Kharagpur. In next phase, about 9,600 teachers from different colleges were taught online by these three faculties and assisted by us again through a 1-week workshop. As an assistant, I took some tutorials, prepared and evaluated assignments, answered quires of the participants in both the workshops.

As Guest Instructor: Worked as a guest lecturer at Asutosh College, under the affiliation of University of Calcutta during the period June 2012 to November 2012. I took the courses entitled *Object Oriented Programming* and *Digital Design Lab* for B.Sc (Hons. in Computer Science) third-year and first-year students, respectively.

As Mentor: Mentored four postgraduate students and eight intern students during Ph.D. in IIT

Kharagpur. Currently, I am mentoring two MS students (MS by research) and two Ph.D. students in IIT Kharagpur.

Technical Experience

During my Ph.D., with the help of one Mtech, one MS, and one Btech students of IIT Kharagpur, I have developed a testbed emulating the behavior of a networked control system. The testbed is used both for the research experiments and teaching purpose such as real-setup demonstration, lab assignments. The testbed emulates the plant-control (double integrator plant) models and their behavioral responses in conjunction with its analysis tool which is used to ascertain bounds on control performance of a given controller over a given network, by artificially inducing random or fixed failure rates, packet drops, and external noise either in the network or the physical plant. The details of the testbed can be found in: http://cse.iitkgp.ac.in/∼soumya/mcn/index.html.

References

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