Srobona Mitra **Curriculum vitae**

CONTACT INFORMATION
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OBJECTIVE
Full-time position where I can get hands-on experience on the state-of-the-art verification techniques for industrial-strength designs and exposure towards incorporating new research directions to the industrial context.

AVAILABILITY
- ▷ Start time is negotiable, but preferably March-April 2012
- ▷ Geographic location is flexible, but preferably in Bangalore, India

RESEARCH INTERESTS
Formal, Semi-formal and Post-silicon Verification of Hardware Designs

EDUCATION

Indian Institute of Technology Kharagpur, Kharagpur, India

Ph.D., Computer Science and Engineering — March 19, 2007 - Present

- Thesis Topic: Formal Methods for Effective Verification of Local Design Changes
- Area of Study: Hardware Verification
- Advisors: Professor Pallab Dasgupta and Professor Partha Pratim Chakrabarti

M.Tech., Computer Science and Engineering — July 2004 - June 2006

- CGPA: 9.63 (10.00 scale) (Rank 1)
- Thesis Topic: A framework for battery-aware multiprocessor task scheduling in real-time embedded systems
- Advisor: Professor Anupam Basu
- Thesis Abstract: The aim of the project was to develop a scheduling framework that will assign tasks to processors taking into account inter-task dependencies and deadlines, with the objective of optimizing battery life. We achieved considerable improvement in battery life over existing schemes by the proposed scheduling technique.
- Courses Credited: Advances in Algorithms, High Performance Computer Architecture, Embedded Systems, Machine Learning, Distributed Systems, Cluster and Grid Computing, Data Warehousing and Data Mining, Information and System Security

Faculty of Engg. and Technology, Jadavpur University, Kolkata, India

B.E., Computer Science and Engineering — June 2000 - June 2004

- Percentage: 88.25% (Rank 6)
- Project Topic: Development of a software interface to the performance monitoring hardware of processors
- Advisor: Professor Nandini Mukhopadhyay
- Abstract: I have done a project on building a software interface to the in-built hardware performance counters that are present in Intel Pentium 3, Intel Pentium 4 and Intel Xeon Dual processors. All these processors have performance counters that can count different events related to processor performance.

Refereed Journal Publications

Srobona Mitra, Priyankar Ghosh and Pallab Dasgupta, *"Verification by parts: Reusing Component Invariant Checking Results"*, accepted for publication in *IET Computers & Digital Techniques* journal, June 2011

Srobona Mitra, Ansuman Banerjee, Pallab Dasgupta and Harish Kumar, *"Trace Assisted Formal Methods for the Verification of Bug Fixes"*, communicated to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, September 2011

Srobona Mitra, Ansuman Banerjee, Pallab Dasgupta and Harish Kumar, *"Formal Methods for Ranking Counterexamples Through Assumption Mining"*, Manuscript under preparation

Conference Publications

Srobona Mitra, Ansuman Banerjee and Pallab Dasgupta,*"Formal Methods for Ranking Counterexamples Through Assumption Mining"*, accepted in *Design Automation and Test in Europe (DATE)*, 2012

Anvesh Komuravelli, *Srobona Mitra*, Ansuman Banerjee and Pallab Dasgupta, *"Backward Reasoning with Formal Properties: A methodology for bug isolation on simulation traces"*, in the Proceedings of *Asian Test Symposium (ATS)*, November 2011, pp. 238 -243

Aritra Hazra, *Srobona Mitra*, Pallab Dasgupta, Ajit Pal, Debabrata Bagchi and Kaustav Guha, *"Leveraging UPF-Extracted Assertions for Modeling and Formal Verification of Architectural Power Intent"*, in the Proceedings of *Design Automation Conference (DAC)*, June 2010, pp. 773-776

Srobona Mitra, Antara Ain, Priyankar Ghosh and Pallab Dasgupta, *"A Study of Modeling Techniques in use in Digital and Mixed-Signal Domains for Semi-Formal Verification"*, in the Proceedings of *IEEE TechSym*, April 2010, pp. 103 - 108

Srobona Mitra, Priyankar Ghosh, Pallab Dasgupta and Partha P.Chakrabarti, *"Incremental Verification Techniques for an Updated Architectural Specification"*, in the Proceedings of *IEEE INDICON*, December 2009, pp. 1 - 4

Aritra Hazra, Ansuman Banerjee, *Srobona Mitra*, Pallab Dasgupta, P. P. Chakrabarti and C. R. Mohan, *"Cohesive Coverage Management for Simulation and Formal Property Verification"*, in the Proceedings of *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)* 2008, pp. 251 - 256

Other Conference Publications

Priyankar Ghosh, *Srobona Mitra*, Indranil Sengupta, Bhargab Bhattacharya and Sharad Seth, *"A Hybrid Test Architecture to Reduce Test Application Time in Full Scan Sequential Circuits"*, in the Proceedings of *IEEE INDICON*, December 2009

Priyankar Ghosh, *Srobona Mitra* and Pallab Dasgupta, *"A Novel Methodology to Assist Client Side Testing of Interactive Web Applications"*, in the Proceedings of *International Conference on Information Technology (ICIT)*, December 2009

Anirban Lahiri, Anupam Basu, Monojit Choudhury and *Srobona Mitra*, *"Battery-aware Code Partitioning for a Text to Speech System"*, in the Proceedings of *Design Automation and Test in Europe (DATE)* 2006, pp. 1 - 6

Posters

Srobona Mitra, Pallab Dasgupta, Sudhindra Pandav and Harish Kumar, *"Trace-Enabled Formal Verification: An Approach for Formal Verification of Post-Silicon Debug and Bug-Fixing"*, accepted in poster session of *Intel India Innovation Day*, March 2011

RESEARCH EXPERIENCE

PhD Research, Dept. of Computer Science and Engineering, Indian Institute of Technology Kharagpur

- Title: Formal Methods for Effective Verification of Local Design Changes
- Abstract: Large digital integrated circuits typically consist of multiple functional units integrated using glue logic. The main functional units in the design are typically extensively verified using both formal and simulation techniques, whereas the glue logic (tribal logic), which accounts for a large fraction of the integrated circuit (40% or above), is not well-documented and not formally verified in industrial practice. The glue logic is often modified locally late in the design cycle for (a) fixing bugs which often appear due to incorrect interpretation of the architecture in specific corner case scenarios, (b) intent modification which is performed later in the design cycle and the component is modified accordingly. Both these two kinds of changes are expected to have local side effects. However, these local changes may indirectly affect a much larger portion of the glue logic, and it is non-trivial to determine the exact boundary of the cone-of-influence of that change. Therefore model checking or sequential equivalence checking on the glue logic in its entirety does not scale. In this research, we propose methodologies for effectively verifying such local design changes at a global level, without attempting to apply formal methods on the entire glue logic.

PROFESSIONAL EXPERIENCE

Sponsored Research and Industrial Consultancy (SRIC), IIT Kharagpur

Designation: Research Consultant

Formal verification of post silicon bug fixes (FVSB)

January 1, 2011 - present

- Sponsored by: Intel Technology India Pvt. Ltd., Bangalore
- Abstract: Objective of this project is to investigate formal methods for automatic extraction of invariants from simulation traces and formal specifications of components. This involves exploring how post-silicon bug traces and pre-silicon simulation dumps can be used for extracting invariants to enhance verification of post-silicon bug fixes with significant degree of confidence.

Leveraging Simulation Dumps and Failure Traces for Formal Property Verification (LSD)

October 1, 2009 - December 31, 2010

- Sponsored by: Intel Technology India Pvt. Ltd., Bangalore
- Abstract: Post-silicon debug often uncovers pre-silicon design errors. Some of these errors are such that post-silicon validation cannot proceed before they are fixed. Sometimes the fix works for the specific scenario uncovered by the debug, but may miss similar (or slightly different) scenarios. Consequently a bug from the same family crops up in the next silicon. The goal of this project is to (a) Formalize the notion of a scenario as a family of traces, (b) Formalize the notion of a bug-family as a set of conditions that enable a family of bug traces, and (c) Formally prove that a bug-fix eliminates a bug-family.

Coverage Metrics for Design Intent Coverage (CMDI)

March 19, 2007 - September 30, 2009

- Sponsored by: Intel Corporation, Santa Clara, USA
- Abstract: I also worked on a research project, which attempted to relate formal verification coverage and simulation coverage in pre-silicon validation. We proposed the use of a

test plan language as a formal basis for unifying the coverage goals for simulation and formal property verification. We present methods for computing the coverage of test points individually through simulation and formal property verification and for using the coverage due to one to ease the verification effort on the other.

Additional Project: Formal Methods for Power Intent Verification in Multi-Voltage Designs

- Sponsored by: Synopsys Inc., Bangalore
- Abstract: This project involves formal methods in power intent verification of multi-voltage designs. With the rapid change in low power design and power management policies, the verification of power-managed designs has become a major challenge. To alleviate the problem of verifying power-managed designs, new formats like UPF and CPF have been standardized for expressing the power intent of a design. Given the power intent specification and the logic of the power management strategy, this project attempts to develop formal methods for verifying whether the control signals specified in the power intent are applied in the correct way by the power management logic.

Intel Technology India Pvt. Ltd., Bangalore, India
Designation: Research Intern

Platform Validation Engineering (PVE) Team
February 22, 2010 - September 22, 2010

- Role: Objective of the internship was to deploy the prototype tool I had developed for finding related bugs of same family or verifying a bug fix to be a robust fix for a hardware design (in project LSD), on a module of the actual Intel RTL. The learnings were the scalability issues involved in scaling to industrial-size processor design.

IXIA Technologies Pvt. Ltd., Kolkata, India
Designation: Software Engineer, Development

IxLoad Development Team
June 22, 2006 - March 15, 2007

- Role: I have worked as development engineer in the Video Team of the network testing product IxLoad. The domain of work includes layers 4 to 7 in networking domain.
- Responsibility: I worked on enhancement support of existing features and on developing new features of this product.

Prototype Tools Developed

Enhanced BDD-based Sequential Equivalence Checker (ESeqCheck):

- This tool does backward reachability-based sequential equivalence checking (SEC) on hardware designs using implicit representation of design state space with binary decision diagrams (BDD).
- The main feature of this tool is that in large hierarchical designs, it reuses the reachability information of component state spaces from proven component invariants, to enhance the proof of global invariants, in terms of both time and memory.
- It can effectively prove the sequential equivalence of composite designs after bug fix, to their previous versions, as established by experimental results on various benchmark circuits.
- Takes input designs in flattened netlist format, like BENCH or AIGER format.

Bug Fix Verifier (BFV):

- Given a buggy trace, this tool does a local analysis of the bug, using the given test-bench and the RTL of the design, using dynamic slicing techniques as in software verification domain. The outputs of this tool are the following:
  - A classification of the local signals of the design with respect to their relevance in causing the bug into critical supporting/supporting/indifferent for the bug manifestation.
  - From this analysis outputs those signals which characterize the bug family, that is, whose valuations can cause different related bugs.
- Given the fixed design with respect to this bug, the tool does the following:
  - Formally guarantees that the bug has eliminated this bug family, or
  - If this bug has been eliminated, but related bugs remain, then does analysis to output the set of signals which are to be looked at for debugging further, that is, which are critical supporting or supporting for the bug.
- Takes the design in Verilog, can support a limited subset of Verilog for its analysis. Has been deployed on the cache coherence test case available in the Texas 97 benchmark suite.

Counterexample Ranking tool (GENRANKCEX):

- While proving a property on a deeply embedded logic, the property is model-checked locally on a smaller component module of the design, instead of the entire design, due to scalability issues. But since the inputs of the smaller module are taken as unconstrained, the counterexamples returned by the model-checker may be spurious ones. Objective of this tool is to assign ranks to the counterexamples thrown up by the model-checker, so that the higher ranked counterexamples are more likely to be real in the entire design and the design engineer can look at those and try to reproduce them for debugging with more confidence.
- Ranking is based on assume properties mined from available simulation traces of the entire design.
- Takes as input a design in structural Verilog, and a component of it marked out, and a property on the component. Outputs top ten highest ranked counterexamples for the design.
- Presently has been deployed on hardware benchmark circuits.

TEACHING EXPERIENCE

Dept. of Computer Science and Engineering, IIT Kharagpur

Teaching Assistantship: I have been responsible for grading assignments and class test scripts, taking the tutorial classes and answering student queries. Have also taught certain topics in these courses in occasion of the absence of the teacher in question. I have been TA for the following courses offered in the Department during the course of my PhD tenure:

- Foundations of Computing Science
- Programming and Data Structures Theory
- Advanced Graph Theory
- Distributed Systems
- CAD for VLSI
- Artificial Intelligence
- Algorithms

Have taught the following topics during TA duties to students:

- Model Checking

- Temporal Logics
- Constraint Satisfaction Problems
- List Processing Language LISP
- PROLOG
- Neural Networks

Lectures at the summer course on VLSI: I have presented lectures on *Model Checking* for the summer course on VLSI, organized by the *Advanced VLSI Design Laboratory*, IIT Kharagpur in the two consecutive years 2009 and 2010.

Achievements and Awards

- Was selected as one of 24 finalists from among 200 applicants in the *Google India Women in Engineering Award 2010*. Was a distinguished Conclave invitee for the Google India Women in Engineering Conclave 2010, held on 25th and 26th February 2010, at Google Hyderabad.
- I won the Institute Silver Medal in IIT Kharagpur for acquiring the 1st rank in M.Tech (CS) 2006.
- GATE score of 99.72 percentile (All India Rank 97) in 2004.
- 30th Rank in the West Bengal Joint Entrance Examination 2000.
- Qualified for National Scholarship in both Madhyamik Pariksha 1998 (91.25%) with state rank 28, and Higher Secondary Examination, 2000 (92%) with state rank 24.

Professional Activities

- Presented *"Backward Reasoning with Formal Properties: A methodology for bug isolation on simulation traces"*, at the *Asian Test Symposium (ATS)* Conference, November 2011, held at New Delhi.
- Presented *"Trace-Enabled Formal Verification - An approach for Formal Verification of Post-Silicon Debug and Bug-Fixing"* at *Intel Technology India Pvt. Ltd., Bangalore* in August 2010.
- Presented *"A Study of Modeling Techniques in use in Digital and Mixed-Signal Domains for Semi-Formal Verification"*, at the *IEEE TechSym* Conference, April 2010, held at IIT Kharagpur.
- Reviewer for *Design Automation Conference (DAC)*.

Computing Skills

Programming Languages: C, C++, Verilog, SystemVerilog

Operating Systems: Linux, Windows, Solaris

Tools:

- General Coding Tools: cscope, ctags, gdb
- Circuit Simulator Tool: Spice circuit simulator
- Network Analyzer Tool: Ethereal Network Analyzer
- Formal Property Verification Tools: vis (CU Boulder), ABC (Berkeley USA), NUSMV (CMU), Magellan (Synopsys), IFV (Cadence)
- RTL Simulator Tool: VCS simulator (Synopsys)
- BDD Package: Cudd (Colorado University USA)
- SAT Solver: zChaff (Princeton University USA)

References

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