# Mid Semester Examination

*IIT Kharagpur, CSE Dept., Spring'16*

(CS60058) FAULT TOLERANT SYSTEMS (Full marks = 50)

Answer all questions. In case of reasonable doubt, make practical assumptions

1. Consider a TMR that produces a one-bit output. The characteristics of each of the units are as follows.

   - Unit 1 is either perfectly functional or is stuck at 1,
   - Unit 2 is either perfectly functional or is stuck at 0,
   - Unit 3 is either perfectly functional or is stuck at 0 or 1,
   - The voter never fails.

   Failures that cause the output of a unit to be permanently stuck at 0 or stuck at 1 occur at constant rates $\lambda_0$ and $\lambda_1$, respectively. At time $t$, you carry out a calculation whose correct output is 0. What is the probability that the TMR will produce the correct result ? (Assume that stuck-at faults are the only ones that the system can suffer from, and that these are permanent faults; once a unit has its output stuck at some logic value, it remains stuck at that value forever). **[10]**

2. Write the expression for the reliability of a 5MR system and calculate its MTTF. Assume that failures occur as Poisson processes with rate $\lambda$ per node, that failures are independent and permanent, and that the voter is failure-free. **[10]**

3. Consider a 7 unit system where 2 units are faulty and the original source (among these 7) is not faulty. Explain with example how the *Interactive Consistency Conditions* hold for such a setup while executing the Byzantine General's algorithm. What are the different errors that a watchdog processor can detect while monitoring the system bus between main CPU and memory ? **[7+3]**

4. How many parity bits are required for implementing single error correction of 10 data bits ? Among even and odd parity, what is a better choice for implementing a single parity bit for 10 data bits in a situation where *all bits stuck at 1* is the most llikely error scenario ?[1] Write expressions for the upper and lower bounds and the exact reliability of the non series/parallel system shown in Figure 1. The reliability of module $i$ is denoted by $R_i(t)$. Assume that $D$ is a bi-directional unit. **[2+2+6]**

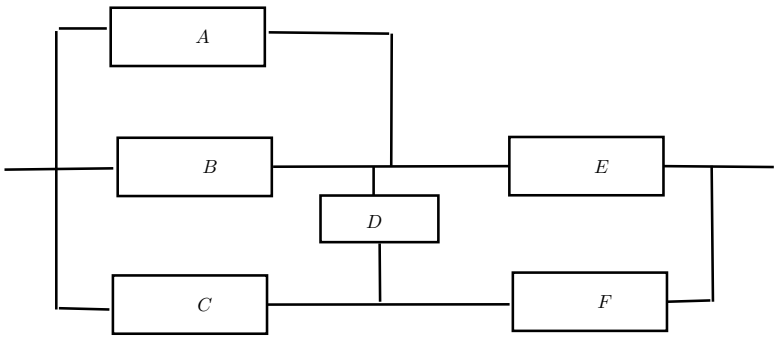


Figure 1: A 6 module non-series/parallel system

5. Contruct the Markov model for a redundant system implementation having one active unit, two inactive spare units and a fault detection and reconfiguration unit which is never at fault. Any unit level failure occurs at rate $\lambda$ and any failed unit is repairable at rate $\mu$. The probability of successful fault detection followed by reconfiguration is $c$. From the model, create the system of equations for rate of change of probability of each state. (you need not solve the equations) **[5+5]**

[1] You need to provide suitable justification