CS60058 - assignment 1

Consider a sequence detector circuit which detects the sequence '1101' and outputs 1 each time it detects the sequence and 0 at all other times. It also detects overlapping sequences.

Assumptions for the perfect circuit

- Use only 6 logic units, 2 of which are flipflops, rest are basic gates.

- One gate has 3 inputs while all other gates are 2 input.

- Use gray code state assignment while designing the circuit.

Assumptions about possible faults

- The output of each logic gate can have stuck at 0 or stuck at 1 fault with the following probabilities. In your design you can number the gates as per your

Gate No.	Stuck at 0	Stuck at 1
1	0.1%	0.2%
2	0.5%	0.3%
3	0.5%	0.4%
4	5%	3%

choice.

- At any instance, only one logic gate can be faulty.

- Flipflops are fault-free.

TODO You have to measure the failure probability of this circuit using simulation based analysis. This can be done as follows.

- Create Verilog module for the perfectly running circuit. Create Verilog modules for all the possible faulty modes of operation of the circuit. Take the outputs of all modules and pass through a multiplexer.

- Write a suitable test-bench that automatically provides inputs for the multiplexer select lines and generates random circuit inputs for very large number of simulations (> 10000) while respecting the probabilities of faults as mentioned.

- Incorporate a comparator which compares the system output with the perfect output in each run and accordingly counts the total number of failure scenarios.

- Submit a 1 page report describing 1) your design and 2) input generation method. Also report the % failure of the circuit as analysed by your simulation setup.

Submission Guidelines : DO NOT copy code from others. We will use Moss to automatically check for evidence of plagiarism.