(CS60058) FAULT TOLERANT SYSTEMS

IIT Kharagpur, CSE Dept., Spring'15

Mid Semester Examination (Full marks = 60)

Answer any six questions. In case of reasonable doubt, make practical assumptions.

1. Consider two processors P_1 and P_2. Each processor P_i (i=1,2) places its request on a queue Q_i which is sampled by an unbiased switch that keeps on alternating among the two queues every cpu cycle. When the switch is at position i, any request placed in queue Q_i by processor P_i in that cpu cycle or earlier is serviced instantaneously. In every cpu cycle, if there is no pending memory access request due to processor P_i, it generates a new request with probability p_i. Derive a DTMC model for the system where you clearly explain the intuition behind each state and compute the steady state probabilities. **[7+3]**

2. Prove that a TMR system has higher reliability than simplex only for short mission times. Explain the idea behind TMR-simplex scheme and formulate the resulting reliability expression. **[6+4]**

3. (a) Prove that the MTTF of a parallel system with all its modules having failure rate λ is given by $\sum_{k=1}^{N} \frac{1}{k\lambda}$. **[5]**
   (b) Prove that a butterfly network with a single extra stage can tolerate one switchbox failure anywhere in the network. **[5]**

4. (a) Prove that a butterfly network with a single extra stage cannot tolerate more than one simultaneous switchbox failure. **[5]**
   (b) Consider a permanent fault which has occurred in some specific cache block inside a processor. Disabling the entire faulty cache will significantly degrade performance. Hence, it makes sense to use error detection codes to identify which cache block has suffered a permanent fault. In that case, the *faulty-bit* of a block will be set once the block is identified as faulty. When access to that certain address of cache occurs, the cache control logic makes use of the faulty-bit by treating the access as a miss and also excludes the block from the cache replacement algorithm. Discuss the impact of such a scheme on the system performance degradation for different cache configurations (direct mapped, set associative, fully associative etc.) **[5]**

5. Consider a triplex that produces a one-bit output. Failures in each individual module is any one of the following types: permanently stuck at 0 or permanently stuck at 1; occurring at constant rates λ_0 and λ_1 respectively. The voter never fails. i) Compute the probability of a single module being stuck at 0 at any time inside [0, t]. ii) At time t, you carry out a calculation whose correct output is 0. What is the probability that the triplex will produce an incorrect result? **[5+5]**

6. (a) Derive all codewords for the separable 5-bit cyclic code based on the generating polynomial X + 1 and compare the resulting codewords to those for the non-separable code. **[5]**
   (b) Show that the Hamming distance of an M-of-N code is 2. **[3]**
   (c) To an n-bit word with a single parity bit (i.e., a total of (n + 1) bits), a second parity bit for the (n+1)-bit word has been added. How would the error detection capabilities change? **[2]**

7. For a RAID3 system with d data disks and one parity disk each having failure rate λ and repair rate μ, construct a Markov model and compute the MTTDL. **[5+5]**