Design Verification – *Overview*

Testing & Verification

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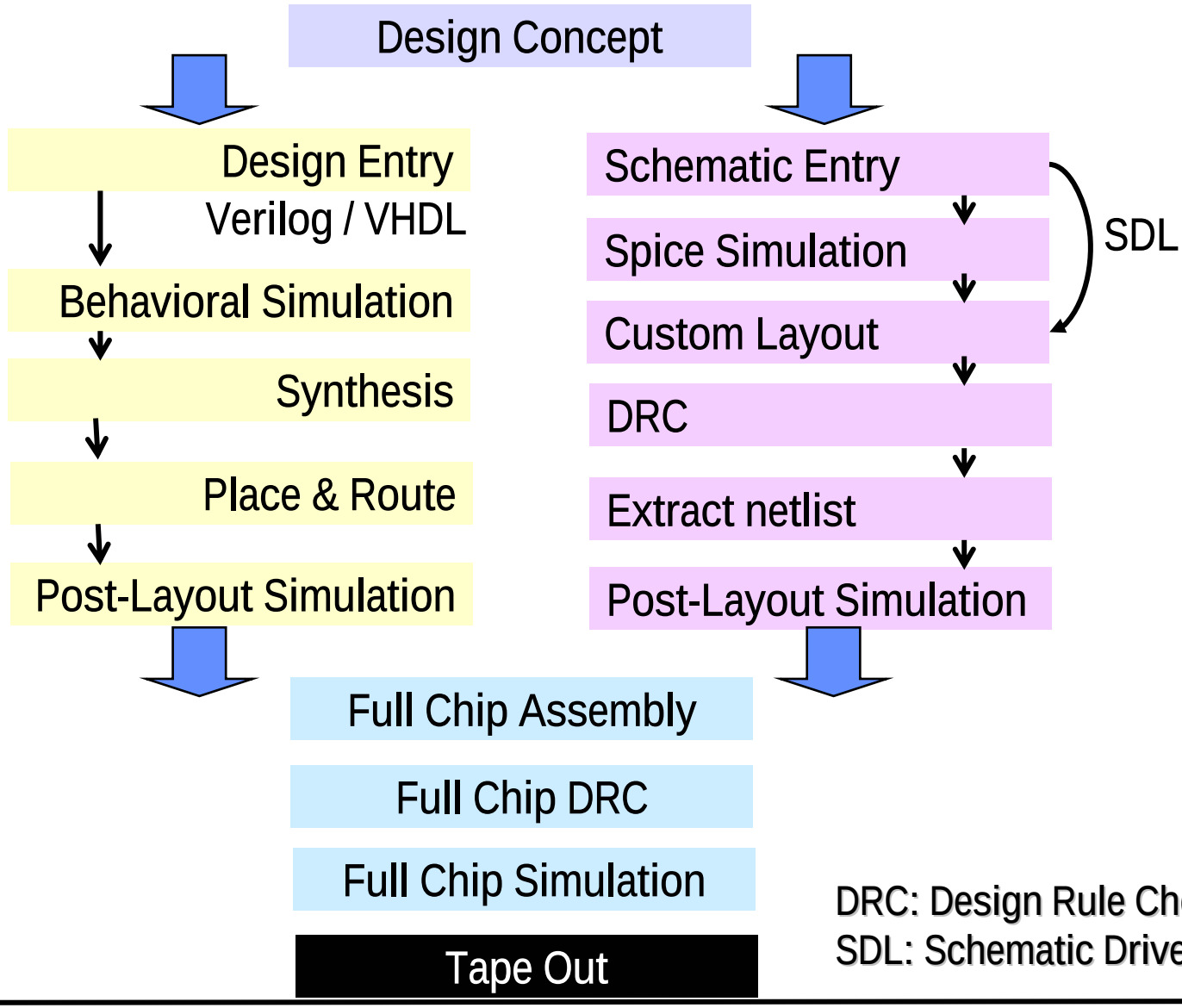
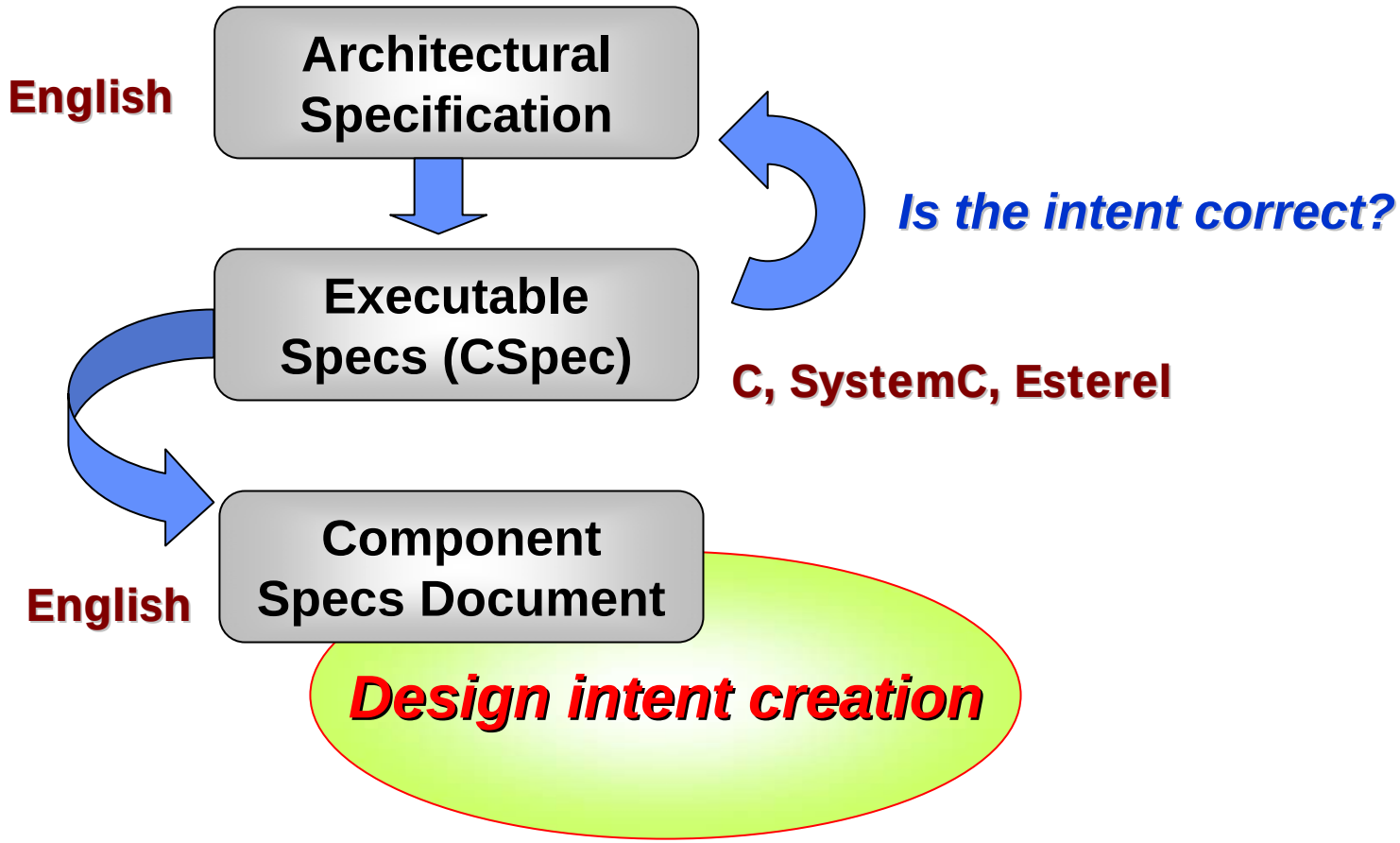
Design Flows: *Digital versus Analog*

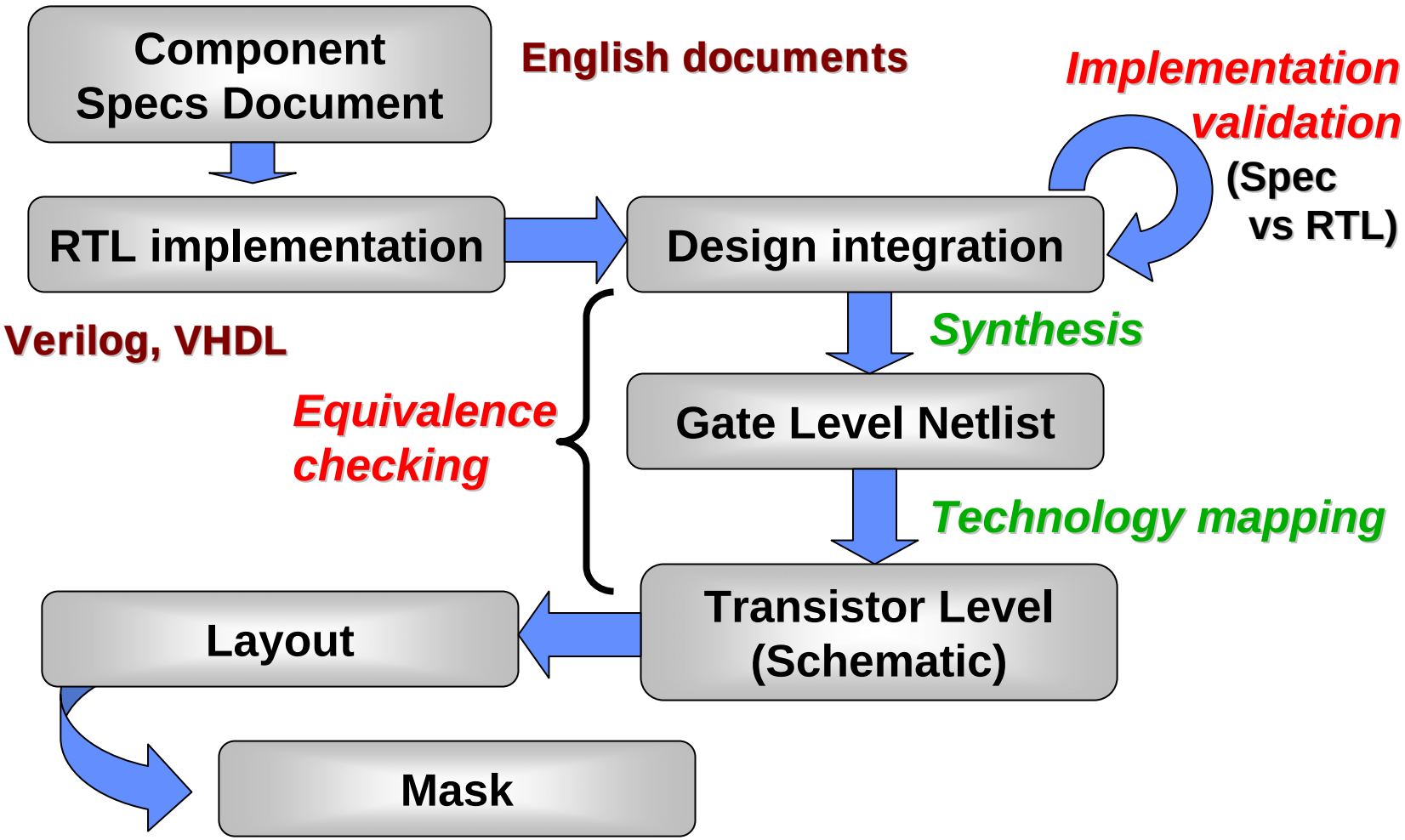


DRC: Design Rule Checking
SDL: Schematic Driven Layout

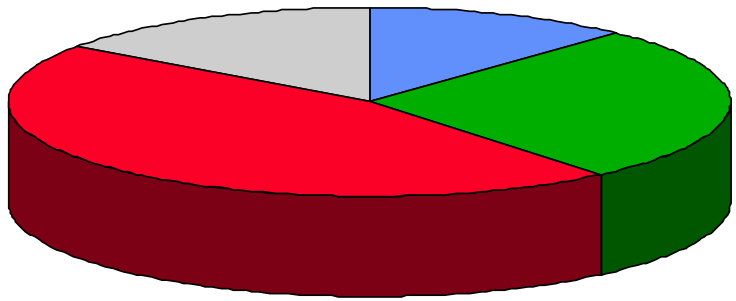
Design Cycle: *Intent Creation*



Design Cycle: *Implementation*



Verification Dominates Design



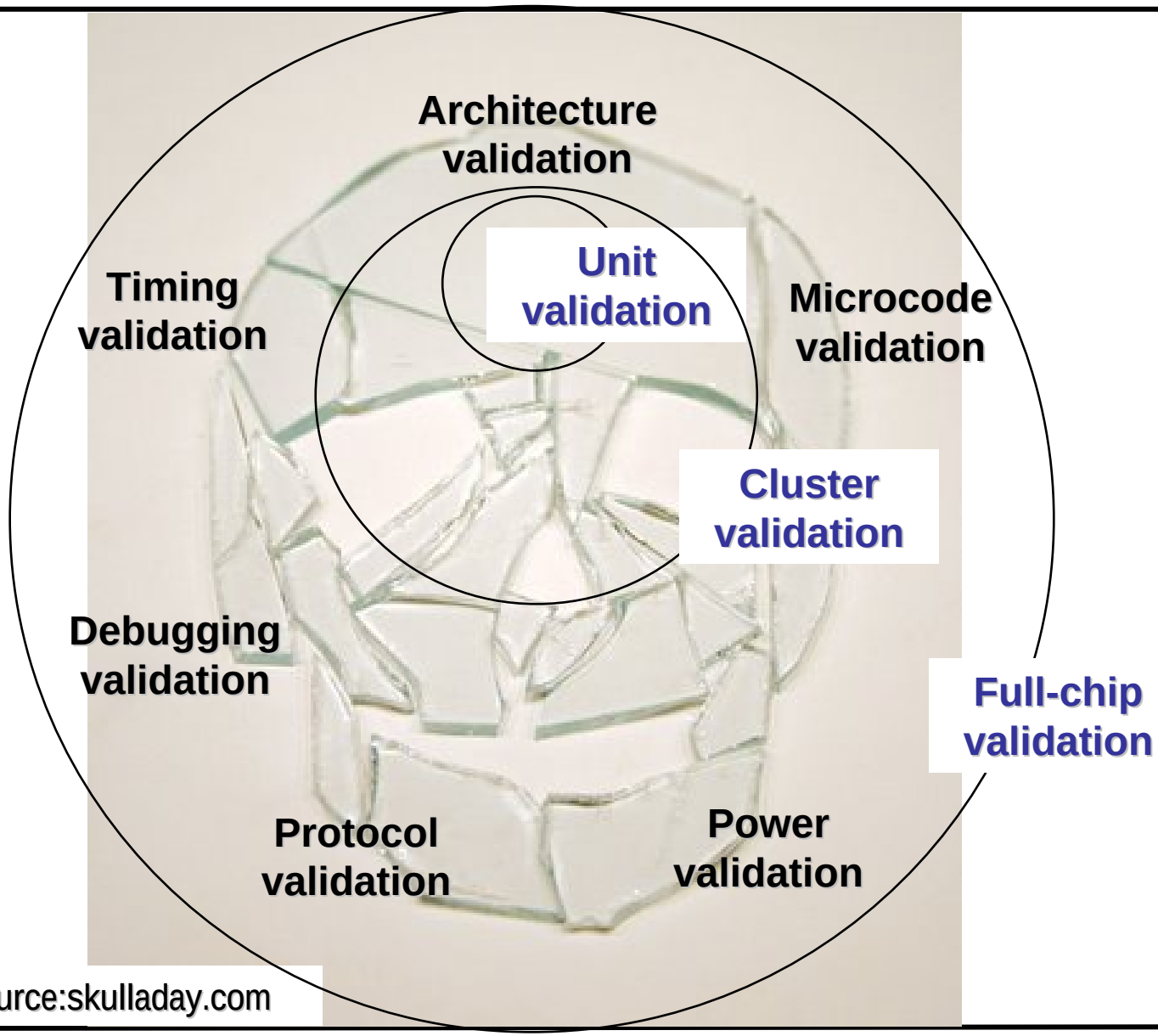
- Synthesis
- Timing analysis
- Equivalence checking
- DFT

- High-level design
- RTL coding
- Block-level simulation

- Behavioral modeling
- Architecture level simulation
- System level simulation

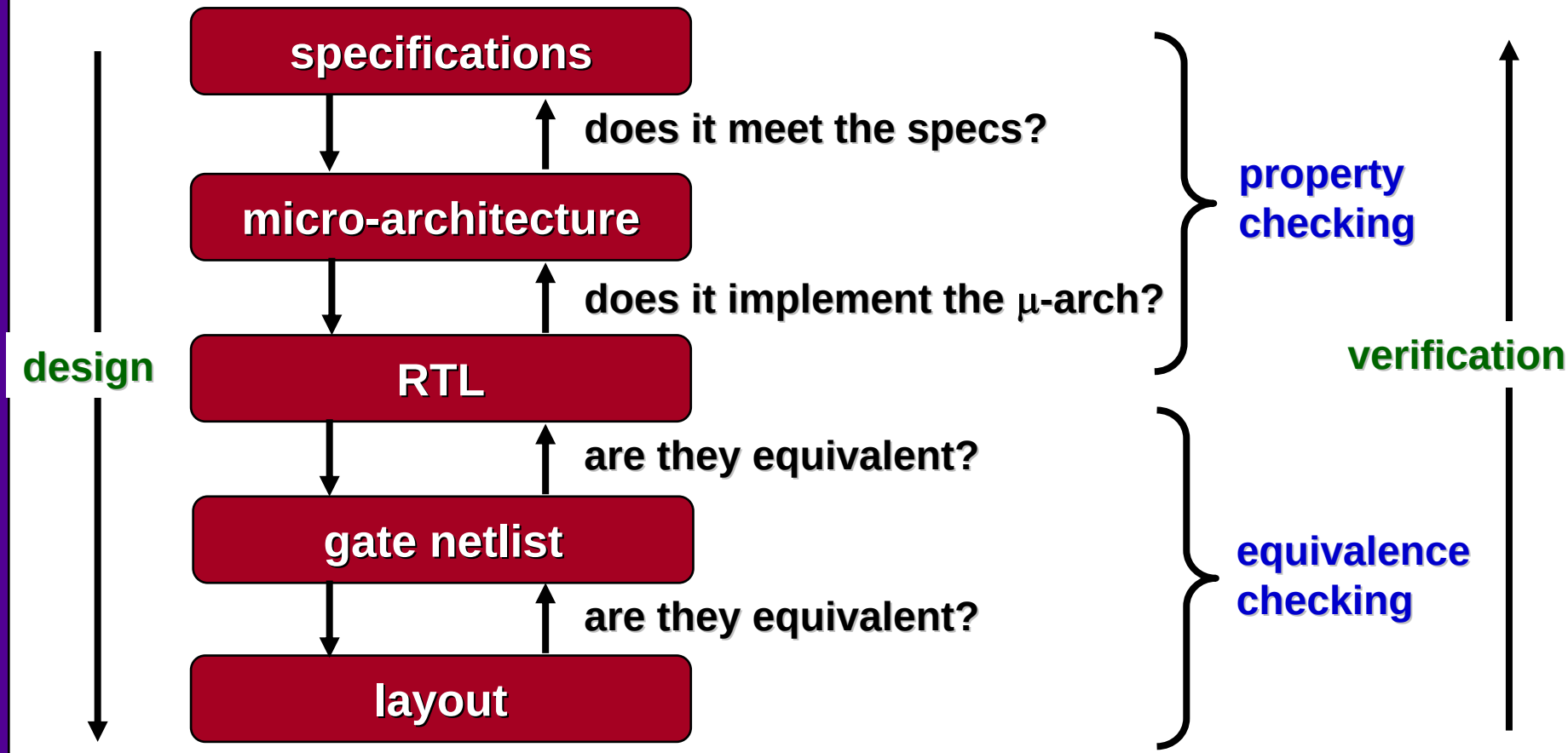
Source: 0-In Design Automation

Pieces of the verification puzzle



Picture source:skulladay.com

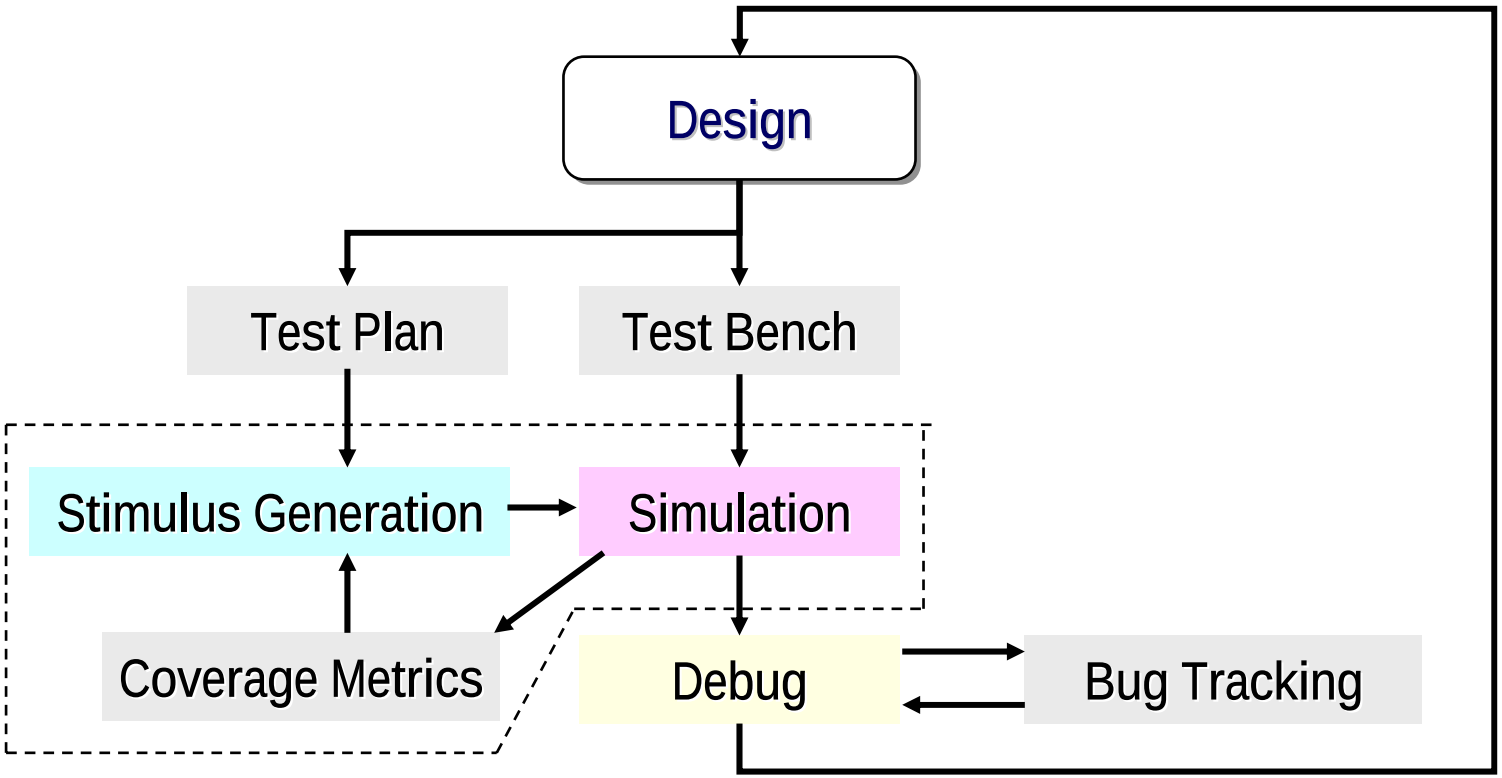
Design and Verification



Functional Verification Challenge

- **Is the implementation correct?**
  - **How do we define *correct*?**
    - **Classical: Simulation result matches with golden output**
    - **Formal: Equivalence with respect to a golden model**
    - **Property verification: Correctness properties (assertions) expressed in a formal language**
      - **Formal: Model checking**
      - **Semi-formal: Assertion-based verification**
  - **Trade-off between computational complexity and exhaustiveness**

Simulation



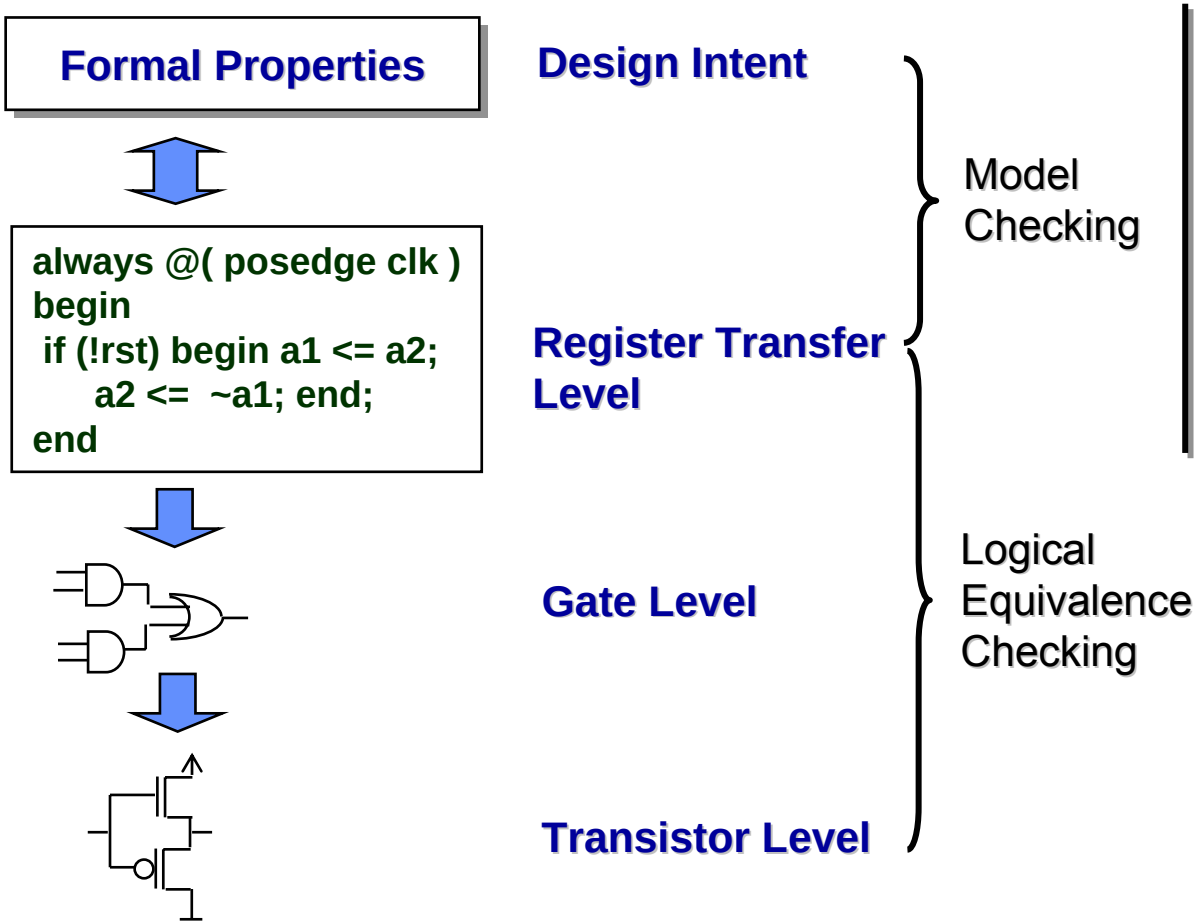
Advances:

- Test bench languages are richer (such as SystemVerilog)
- Coverage monitors and assertions
- Layered test benches and Transaction Level Modelling

Advent of Formal Methods in EDA

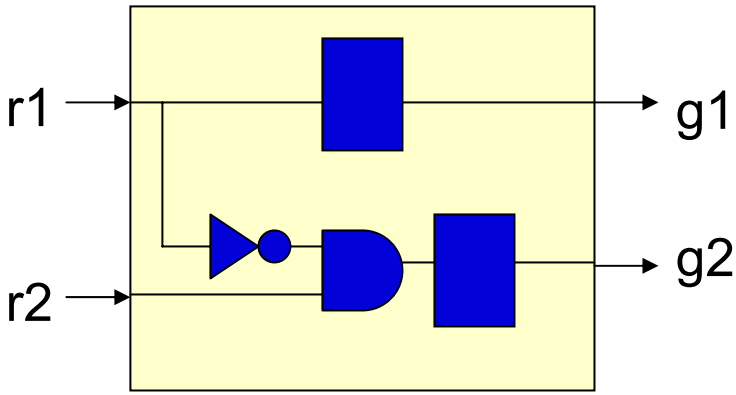
Goal: ***Exhaustive verification of the design intent within feasible time limits***

Philosophy: ***Extraction of formal models of the design intent and the implementation and comparing them using mathematical / logical methods***



- Temporal Logics
  (*Turing Award: Amir Pnueli*)
- Adopted by Accelera / IEEE
- Integrated into SystemVerilog
- Tools:
  Academia: NuSMV, VIS
  Industry: Magellan (Synopsys)
  IFV (Cadence)
- 2008: Clarke & Emerson get Turing Award

Toy example: Priority Arbiter



- Either g1 or g2 is always false (mutual exclusion)

$$G[\neg g1 \vee \neg g2]$$

- Whenever r1 is asserted, g1 is given in the next cycle

$$G[\, r1 \Rightarrow Xg1 \,]$$

- When r2 is the sole request, g2 comes in the next cycle

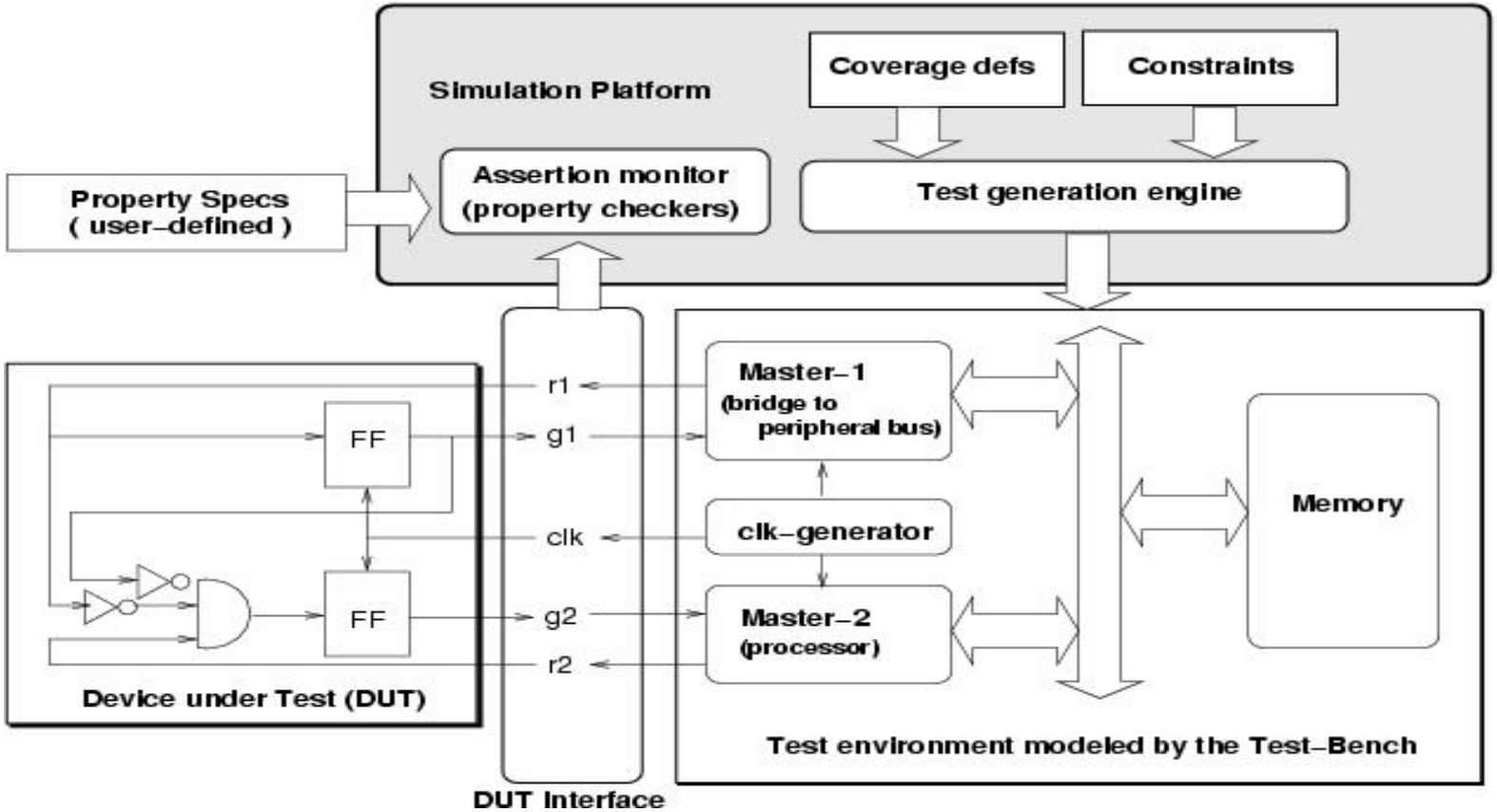
$$G[\, (\neg r1 \wedge r2) \Rightarrow Xg2 \,]$$

- When none are requesting, the arbiter parks the grant on g2

$$G[\, (\neg r1 \wedge \neg r2) \Rightarrow Xg2 \,]$$

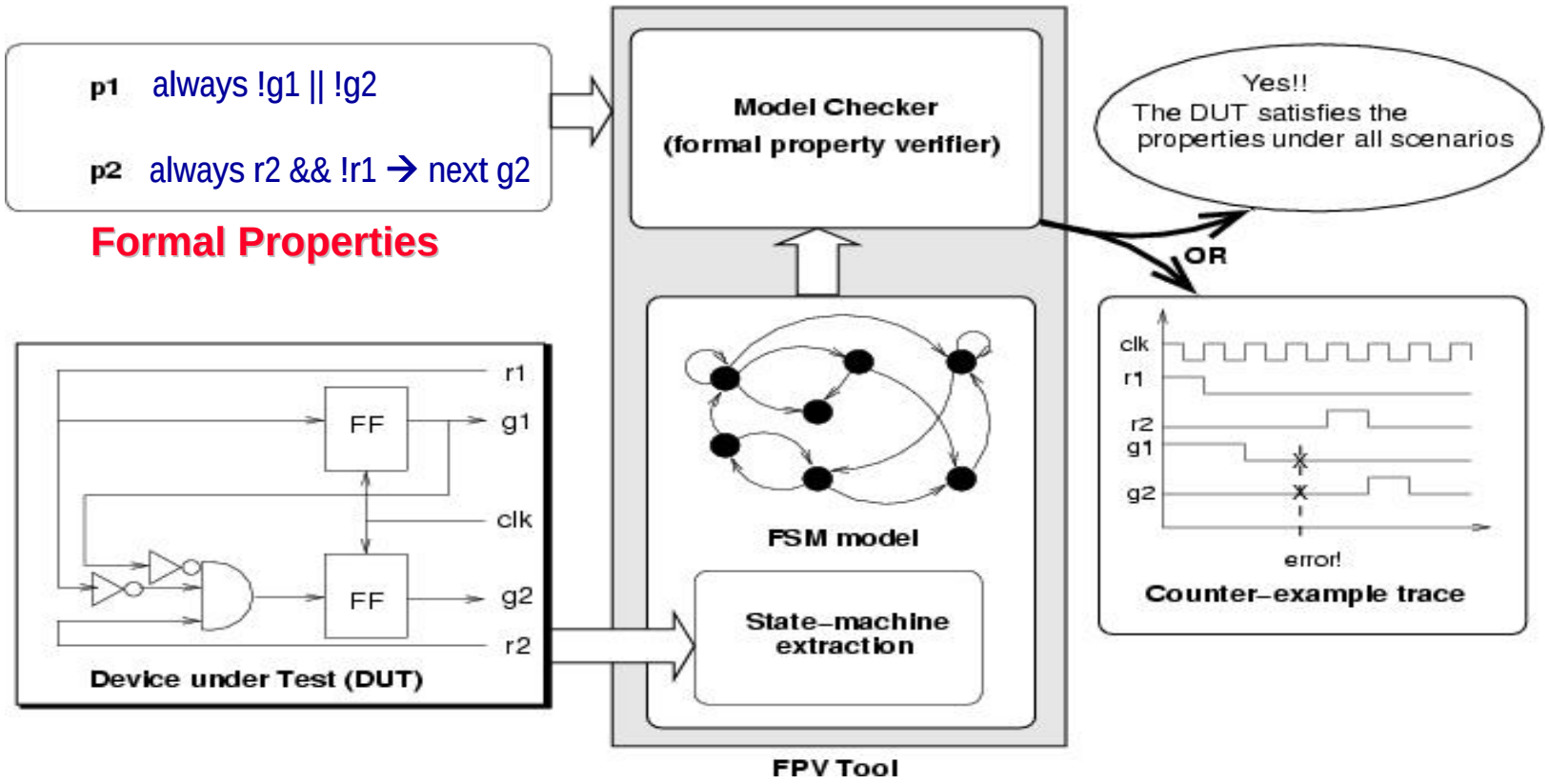
Violation!!

Dynamic Property Verification (DPV)



[Source: *A Roadmap for Formal Property Verification, Springer, 2006*]

Formal Property Verification (FPV)

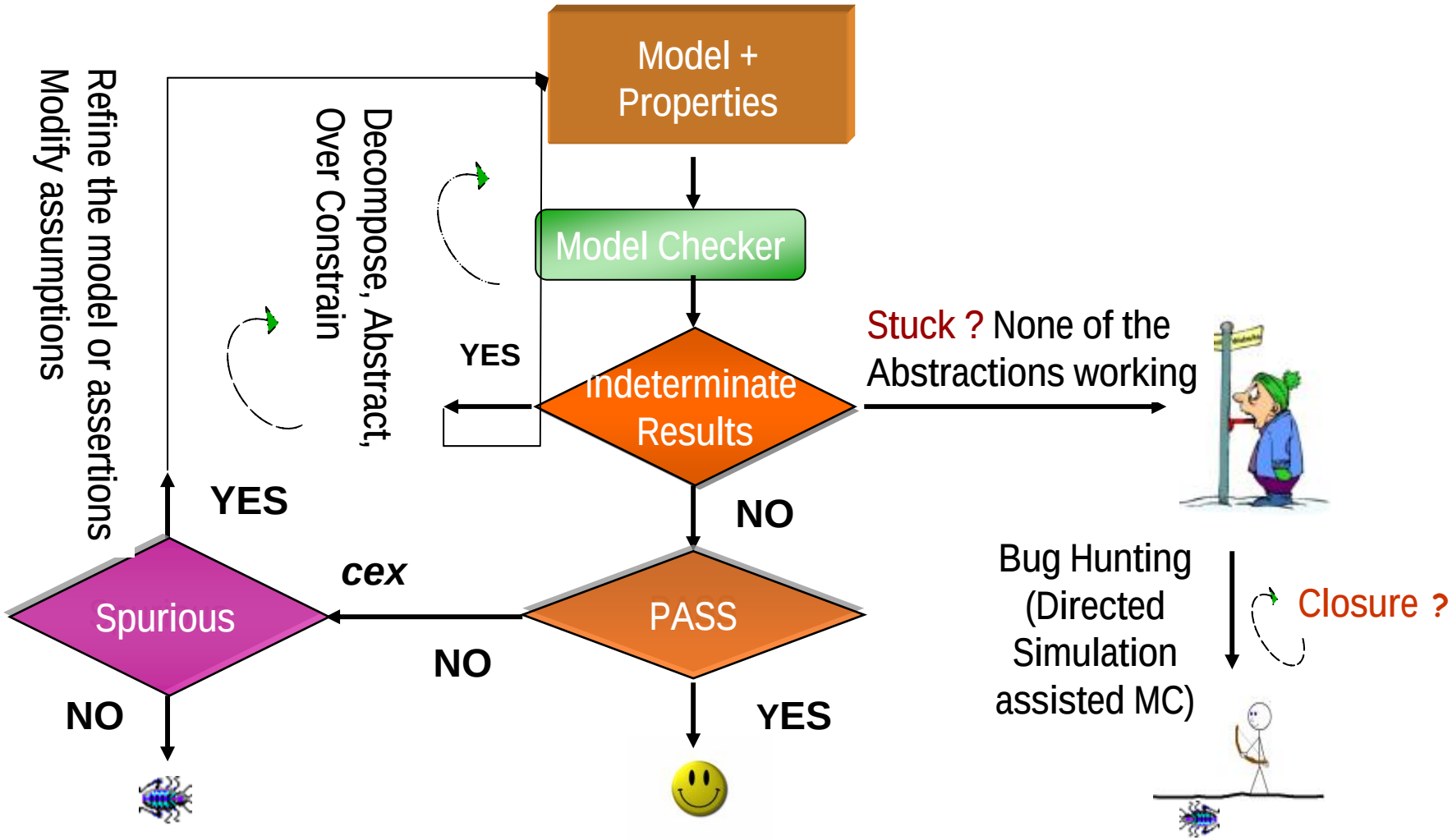


Temporal Logics (Timed / Untimed, Linear Time / Branching Time): ***LTL, CTL***

Early Languages: ***Forspec (Intel), Sugar (IBM), Open Vera Assertions (Synopsys)***

Current IEEE Standards: ***SystemVerilog Assertions (SVA),***
Property Specification Language (PSL)

Assertion Based Verification Flow



[Source: Raj Mitra, TI]

Course Agenda: *Verification Track*

- Design Entry: *Brief overview of Verilog*
- Simulators: *How they work*
- Test Scenarios and Coverage
- Static Checks
- Symbolic Representation of Logic and State Spaces: *BDDs, SAT*
- Equivalence Checking
- Assertions
- Formal Property Verification: *Model Checking*
- Formal Verification Coverage

Verification Group Profile

The verification research group focuses on providing industrially relevant methods for the verification of various designs – ranging from digital and mixed-signal chip designs to complex software and embedded systems such as automotive control systems. Areas of strength include:

- **Design Intent Verification**
- **Formal Verification Coverage**
- **Mixed-signal Design Verification**
- **Coverage-driven Semi-Formal Verif.**
- **Verification of Automotive Systems**
- **Verification of Web Interfaces**

Home: http://www.facweb.iitkgp.ernet.in/~pallab/forverif.html

Research Partners / Sponsors:

DST Govt. of India

The Family

PhD Students:

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Prasenjit Basu (Submitted)
Sayantan Das (Completed)
Ansuman Banerjee (Submitted)
Suchismita Roy (Submitted)
Bhaskar Pal (Submitted)
Arijit Mondal (Ongoing)
P.V. Rajkumar (Ongoing)
Manoj Dixit (Ongoing)
Srobona Mitra (Ongoing)
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Subrat Panda (Ongoing)
Dipankar Das (Ongoing)

MS Students:

Ansuman Banerjee (Completed)
Bhaskar Pal (Completed)
Pritam Ray (Completed)
Arijit Mondal (Completed)
Sayak Ray (Submitted)
Anindyasundar Nandi (Submitted)
Rajdeep Mukhopadhyay (Ongoing)
Aritra Hazra (Ongoing)
Sourashis Das (Ongoing)
Kamalesh Ghosh (Ongoing)
Antara Ain (Ongoing)

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Sagar Chaki (CMU), Arindam Chakraborty (UC Berkeley),
Krishnendu Chakraborty (UC Berkeley), S Sriram (Stanford),
Jayanta Bhadra (U Texas, Austin)

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