Design Flows: Digital versus Analog

- **Design Concept**
  - Design Entry
    - Verilog / VHDL
  - Behavioral Simulation
  - Synthesis
  - Place & Route
  - Post-Layout Simulation

- **Schematic Entry**
  - Spice Simulation
  - Custom Layout
  - DRC
  - Extract netlist
  - Post-Layout Simulation

- **Full Chip Assembly**
- **Full Chip DRC**
- **Full Chip Simulation**

**Tape Out**

**SDL:** Schematic Driven Layout

**DRC:** Design Rule Checking
Design Cycle: *Intent Creation*

- **Architectural Specification**
  - Is the intent correct?
  - English

- **Executable Specs (CSpec)**
  - C, SystemC, Esterel

- **Component Specs Document**
  - English

*Design intent creation*
Design Cycle: Implementation

Component Specs Document

RTL implementation

Verilog, VHDL

Design integration

Equivalence checking

Gate Level Netlist

Synthesis

Technology mapping

Implementation validation

(Spec vs RTL)

Layout

Transistor Level (Schematic)

English documents

Mask
Verification Dominates Design

- Simulation: 46%
  - Behavioral modeling
  - Architecture level simulation
  - System level simulation
- Design: 27%
  - High-level design
  - RTL coding
  - Block-level simulation
- Emulation: 15%
- Structural: 12%

• Synthesis
• Timing analysis
• Equivalence checking
• DFT

Source: O-In Design Automation
Pieces of the verification puzzle

- Architecture validation
- Timing validation
- Microcode validation
- Unit validation
- Cluster validation
- Protocol validation
- Power validation
- Full-chip validation

Picture source: skulladay.com
Design and Verification

- specifications
- does it meet the specs?
- micro-architecture
- does it implement the $\mu$-arch?
- RTL
- are they equivalent?
- gate netlist
- are they equivalent?
- layout

property checking

verification

equivalence checking

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Is the implementation correct?

How do we define correct?

- Classical: Simulation result matches with golden output
- Formal: Equivalence with respect to a golden model
- Property verification: Correctness properties (assertions) expressed in a formal language
  - Formal: Model checking
  - Semi-formal: Assertion-based verification

Trade-off between computational complexity and exhaustiveness
Simulation

Advances:
- Test bench languages are richer (such as SystemVerilog)
- Coverage monitors and assertions
- Layered test benches and Transaction Level Modelling
Advent of Formal Methods in EDA

**Goal:** Exhaustive verification of the design intent within feasible time limits

**Philosophy:** Extraction of formal models of the design intent and the implementation and comparing them using mathematical / logical methods

**Formal Properties**

```
always @(posedge clk)
begin
  if (!rst) begin
    a1 <= a2;
    a2 <= ~a1;
  end;
end
```

**Register Transfer Level**

**Gate Level**

**Transistor Level**

**Design Intent**

**Model Checking**

- Temporal Logics (Turing Award: Amir Pnueli)
- Adopted by Accelera / IEEE
- Integrated into SystemVerilog
- Tools:
  - Academia: NuSMV, VIS
  - Industry: Magellan (Synopsys)
  - IFV (Cadence)
- 2008: Clarke & Emerson get Turing Award
Toy example: Priority Arbiter

- Either $g_1$ or $g_2$ is always false (mutual exclusion)
  
  \[ G[\neg g_1 \lor \neg g_2] \]

- Whenever $r_1$ is asserted, $g_1$ is given in the next cycle
  
  \[ G[ r_1 \Rightarrow Xg_1 ] \]

- When $r_2$ is the sole request, $g_2$ comes in the next cycle
  
  \[ G[ (\neg r_1 \land r_2) \Rightarrow Xg_2 ] \]

- When none are requesting, the arbiter parks the grant on $g_2$
  
  \[ G[ (\neg r_1 \land \neg r_2) \Rightarrow Xg_2 ] \]

Violation!!
Dynamic Property Verification (DPV)

[Source: A Roadmap for Formal Property Verification, Springer, 2006]
Formal Property Verification (FPV)

p1 always !g1 || !g2
p2 always r2 && !r1 → next g2

Formal Properties

Temporal Logics (Timed / Untimed, Linear Time / Branching Time): LTL, CTL

Early Languages: Forspec (Intel), Sugar (IBM), Open Vera Assertions (Synopsys)

Current IEEE Standards: SystemVerilog Assertions (SVA), Property Specification Language (PSL)
Assertion Based Verification Flow

- Model + Properties
- Model Checker
- Indeterminate Results
- Stuck? None of the Abstractions working
- Bug Hunting (Directed Simulation assisted MC)
- Closure?

- Spurious
- Passed
- cex

- Refine the model or assertions
- Modify assumptions
- Decompose, Abstract, Over Constrain

[Source: Raj Mitra, TI]
Course Agenda: Verification Track

- Design Entry: *Brief overview of Verilog*
- Simulators: *How they work*
- Test Scenarios and Coverage
- Static Checks
- Symbolic Representation of Logic and State Spaces: *BDDs, SAT*
- Equivalence Checking
- Assertions
- Formal Property Verification: *Model Checking*
- Formal Verification Coverage
Verification Group Profile

The verification research group focuses on providing industrially relevant methods for the verification of various designs – ranging from digital and mixed-signal chip designs to complex software and embedded systems such as automotive control systems. Areas of strength include:

■ Design Intent Verification
■ Formal Verification Coverage
■ Mixed-signal Design Verification
■ Coverage-driven Semi-Formal Verif.
■ Verification of Automotive Systems
■ Verification of Web Interfaces

Home: [http://www.facweb.iitkgp.ernet.in/~pallab/forverif.html](http://www.facweb.iitkgp.ernet.in/~pallab/forverif.html)

Research Partners / Sponsors:

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# The Family

## PhD Students:
- J.K. Deka (Completed)
- Prasenjit Basu (Submitted)
- Sayantan Das (Completed)
- Ansuman Banerjee (Submitted)
- Suchismita Roy (Submitted)
- Bhaskar Pal (Submitted)
- Arijit Mondal (Ongoing)
- P.V. Rajkumar (Ongoing)
- Manoj Dixit (Ongoing)
- Srobona Mitra (Ongoing)
- Priyankar Ghosh (Ongoing)
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- Subrat Panda (Ongoing)
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## MS Students:
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- Aritra Hazra (Ongoing)
- Sourashis Das (Ongoing)
- Kamalesh Ghosh (Ongoing)
- Antara Ain (Ongoing)

## Some Alumni:
- Shuvendu Lahiri (CMU), Pankaj Chauhan (CMU)
- Sagar Chaki (CMU), Arindam Chakraborty (UC Berkeley), Krishnendu Chakraborty (UC Berkeley), S Sriram (Stanford), Jayanta Bhadra (U Texas, Austin)

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