

CONTACT  
INFORMATION

Department of Computer Science and Engineering  
Indian Institute of Technology Kharagpur  
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RESEARCH  
INTERESTS

Formal Verification, Formal Methods, Program Analysis.

EDUCATION

**Indian Institute of Technology Kharagpur**

Ph.D., Computer Science and Engineering **2010 - 2016**

- Supervisors: Prof. Chittaranjan Mandal and Prof. Dipankar Sarkar
- Thesis Topic: Translation Validation of Optimizing Transformations of Programs using Equivalence Checking
- GPA: 9.28/10 (based on courses taken)

**Heritage Institute of Technology** (West Bengal University of Technology)

B.Tech.(Honors), Computer Science and Engineering **2004 - 2008**

- GPA: 8.49/10
- Supervisor: Prof. Nabanita Das, Indian Statistical Institute, Kolkata
- Bachelor Thesis: TDMA Scheduling in Wireless Sensor Networks
- Worked in the project **Housing Loan Management Systems** sponsored by National Insurance Company Ltd.

PUBLICATIONS

**Journals**

1. Soumyadip Bandyopadhyay, Dipankar Sarkar, Chittaranjan Mandal, **Kunal Banerjee**, Krishnam Raju Duddu.  
A Path Construction Algorithm for Translation Validation using PRES+ Models.  
*Parallel Processing Letters (PPL)*, (accepted).
2. **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.  
Extending the FSM D Framework for Validating Code Motions of Array-Handling Programs.  
*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 33, no. 12, 2014, pages: 2015–2019.
3. **Kunal Banerjee**, Chandan Karfa, Dipankar Sarkar, Chittaranjan Mandal.  
Verification of Code Motion Techniques using Value Propagation.  
*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 33, no. 8, 2014, pages: 1180–1193.
4. Chandan Karfa, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.  
Verification of Loop and Arithmetic Transformations of Array-Intensive Behaviours.  
*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 11, 2013, pages: 1787–1800.

**Conferences / Workshops**

1. K. K. Sharma, **Kunal Banerjee**, Chittaranjan Mandal.  
Determining Equivalence of Expressions: An Automated Evaluator's Perspective. *Technology for Education (T4E)*, Warangal, India, 2015, pages: 35–36.

2. K. K. Sharma, **Kunal Banerjee**, Chittaranjan Mandal.  
Establishing Equivalence of Expressions: An Automated Evaluator Designer's Perspective. *Mining Intelligence and Knowledge Exploration (MIKE)*, Hyderabad, India, 2015, pages: 415–423.
3. **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.  
A Translation Validation Framework for Symbolic Value Propagation Based Equivalence Checking of FSM-DAs. *Source Code Analysis and Manipulation (SCAM)*, Bremen, Germany, 2015, pages: 247–252.
4. Soumyadip Bandyopadhyay, Dipankar Sarkar, **Kunal Banerjee**, Chittaranjan Mandal.  
A Path-Based Equivalence Checking Method for Petri net based Models of Programs. *International Conference on Software Engineering and Applications (ICSOFT-EA)*, Colmar, France, 2015, pages: 319–329.
5. **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.  
Translation Validation of Transformations of Embedded System Specifications using Equivalence Checking. *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Montpellier, France, 2015, pages: 183–186, (**received Best PhD Forum Paper Award**).
6. **Kunal Banerjee**.  
An Equivalence Checking Mechanism for Handling Recurrences in Array-Intensive Programs. *ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages (POPL): Student Research Competition*, Mumbai, India, 2015, pages: 1–2.
7. **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.  
Deriving Bisimulation Relations from Path Extension Based Equivalence Checkers. *IMPECS-POPL Workshop on Emerging Research and Development Trends in Programming Languages (WEPL)*, Mumbai, India, 2015, pages: 1–2.
8. K K Sharma, **Kunal Banerjee**, Indra Vikas, Chittaranjan Mandal.  
Automated Checking of the Violation of Precedence of Conditions in `else-if` Constructs in Students' Programs. *International Conference on MOOC, Innovation and Technology in Education (MITE)*, Patiala, India, 2014, pages: 201–204.
9. K K Sharma, **Kunal Banerjee**, Chittaranjan Mandal.  
A Scheme for Automated Evaluation of Programming Assignments using FSM-D based Equivalence Checking. *IBM Collaborative Academia Research Exchange (I-CARE)*, Bangalore, India, 2014, pages: 10:1–10:4.
10. Partha De, **Kunal Banerjee**, Chittaranjan Mandal, Debdeep Mukhopadhyay.  
Circuits and Synthesis Mechanism for Hardware Design to Counter Power Analysis Attacks. *Euromicro Conference on Digital System Design (DSD)*, Verona, Italy, 2014, pages: 520–527.
11. **Kunal Banerjee**, Chittaranjan Mandal, Dipankar Sarkar.  
Extending the Scope of Translation Validation by Augmenting Path Based Equivalence Checkers with SMT Solvers. *International Symposium on VLSI Design and Test (VDATE)*, Coimbatore, India, 2014, pages: 1–6.
12. Partha De, **Kunal Banerjee**, Chittaranjan Mandal.  
A BDD based Secure Hardware Design Method to Guard Against Power Analysis Attacks. *International Symposium on VLSI Design and Test (VDATE)*, Coimbatore, India, 2014, pages: 1–2.
13. Chandan Karfa, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal.  
Experimentation with SMT Solvers and Theorem Provers for Verification of Loop

- and Arithmetic Transformations. *IBM Collaborative Academia Research Exchange (I-CARE)*, Delhi, India, 2013, pages: 3:1–3:4, **(received Best Paper Award)**.
14. Partha De, **Kunal Banerjee**, Chittaranjan Mandal, Debdeep Mukhopadhyay. Designing DPA Resistant Circuits Using BDD Architecture and Bottom Pre-charge Logic. *Euromicro Conference on Digital System Design (DSD)*, Santander, Spain, 2013, pages: 641–644.
  15. **Kunal Banerjee**, Chandan Karfa, Dipankar Sarkar, Chittaranjan Mandal. A Value Propagation Based Equivalence Checking Method for Verification of Code Motion Techniques. *International Symposium on Electronic System Design (ISED)*, Kolkata, India, 2012, pages: 67–71.
  16. Soumyadip Bandyopadhyay, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal. Translation Validation for PRES+ Models of Parallel Behaviours via an FSMD Equivalence Checker. *International Symposium on VLSI Design and Test (VDAT)*, Shibpur, India, 2012. Published in Lecture Notes in Computer Science (LNCS), vol. 7373, pages: 69–78.
  17. Chandan Karfa, **Kunal Banerjee**, Dipankar Sarkar, Chittaranjan Mandal. Equivalence Checking of Array-Intensive Programs. *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Chennai, India, 2011, pages: 156–161.
  18. **Kunal Banerjee**, Priyanko Basuchaudhuri, Debesh Sadhukhan, Nabanita Das. A Fair Multiple-Slot Assignment Protocol for TDMA Scheduling in Wireless Sensor Network. *Workshop on Mobile Systems (WoMS)*, Kolkata, India, 2008, pages: 65–71.

PROFESSIONAL  
EXPERIENCE

**Sponsored Research and Industrial Consultancy**, Indian Institute of Technology Kharagpur

Verification of embedded system designs **Jul 2009 - Oct 2012**

- Designation: Senior Research Fellow
- Project Title: Extending the scope of equivalence checking in complex embedded system design verification
- Sponsor: Department of Science and Technology, Govt. of India

**Tata Consultancy Services**, Kolkata

Database management **Nov 2008 - Jun 2009**

- Designation: Assistant System Engineer
- Worked in the database management group for McGraw-Hill Education

TEACHING  
EXPERIENCE

**Indian Institute of Technology Kharagpur**

Teaching Assistant

- Programming and Data Structures (Autumn 2014) for Prof Soumyajit Dey
- Programming and Data Structures (Spring 2014) for Prof Niloy Ganguly
- Discrete Structures (Autumn 2013) for Prof Animesh Mukherjee
- Programming and Data Structures (Spring 2013) for Prof Partha Bhowmick
- Theory of Computation (Autumn 2012) for Prof Goutam Biswas
- Computer Architecture and Operating Systems (Spring 2012) for Prof Dipankar Sarkar
- Formal Systems (Spring 2011) for Prof Sujoy Ghose
- Discrete Structures (Autumn 2010) for Prof Sudeshna Sarkar
- Programming and Data Structures Lab (Spring 2010) for Prof Goutam Biswas

- Computer Organization and Architecture Lab (Autumn 2009) for Prof Indranil Sengupta, Prof Dipankar Sarkar, Prof Chittaranjan Mandal, Prof Debdeep Mukhopadhyay

Instructor

**AVLSI Lab Summer Course 2010**

- Gave a lecture on “Logic Synthesis”
- Student co-ordinator for the digital group

TALKS

- Translation Validation of Transformations of Embedded System Specifications using Equivalence Checking, *Inter-Research-Institute Student Seminar in Computer Science (IRISS)*, Goa, India, 2015.
- Translation Validation of Embedded System Specifications using Equivalence Checking, *Tata Research Development and Design Centre (TRDDC)*, Pune, India, 2014.
- Translation Validation using Path Based Equivalence Checkers Augmented with SMT Solvers, *Formal Methods Update Meeting 2014*, Kharagpur, India, 2014.

AWARDS

- Best PhD Forum Paper Award in the conference ISVLSI 2015
- Best Paper Award in the conference I-CARE 2013
- TCS Research Fellowship 2012

TECHNICAL SKILLS

- Programming: C, C++, Java, PL/SQL, Scheme, Prolog, Lisp, Visual Basic and others along with some scripting and markup languages
- Tools: ACL2, CUDD, CVC, ISL, Yices, Z3
- Languages: Bengali, English, and Hindi

REFERENCES

- Prof. Dipankar Sarkar, ds@cse.iitkgp.ernet.in
- Prof. Chittaranjan Mandal, chitta@iitkgp.ac.in
- Prof. Debdeep Mukhopadhyay, debdeep@cse.iitkgp.ernet.in