Devleena Ghosh

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Education

- **Ph.D.** (Pursuing) in Computer Science and Engineering, IIT Kharagpur
  - Computational biology, Parameter estimation, Formal modelling and verification
  - Supervisor: Prof. Chittaranjan Mandal
- **M.Tech** in Computer Science and Engineering, IIT Kharagpur **2011 - 2013** (Summa Cum Laude) with CGPA **9.78**
- **B.E.** in Computer Science and Technology from IIEST, Shibpur (formerly BESU, Shibpur), West Bengal, India, **2006 - 2010** with average percentage **83.46%**

Research Experience

1. **Developing a tool for application of formal methods in Railway Interlocking**.
   · Objective: An auto generated and optimized formal model of the railway interlocking system was validated against some safety properties. The model was generated from the validated input of yard layout and control table. GROOVE graph grammar tool is used for layout validation, NuSMV used for model checking, and Flex, Bison are used to create parser.
2. **Developing Virtual Lab along with a simulation tool for conduction of experiments in Logic Design and Computer Organization**, in Dept. of Computer Science & Engineering, IIT Kharagpur sponsored by MHRD, India. The developed simulation tool is in use to conduct laboratory courses of under and post-graduate level students at IIT Kharagpur.
   · Objective : To develop a virtual Laboratory package to support the teaching of computer organization and architecture along with an efficient interactive generic simulation platform (using Java). Deployed at : https://cse.iitkgp.ac.in/~chitta/coldvl/
3. **Iris Recognition** as B.E. final year project.
   · Objective : To uniquely recognize a person using biometric authentication technique. The unique information was extracted from some given Iris images by image processing (using C).
4. **Automatic Analysis of PET tumor images for Radiotherapy treatment Planning** as part of internship program in Queens University, Belfast (2008).
   · Objective : Given some PET images of chest cavity, we had to detect the tumor and analyse it depending on the size, shape and position. These results are needed for Radiotherapy Treatment Planning (using MATLAB - image processing tool).

Work Experience

- Worked as a **Software Engineer** (Aug 2013 - Dec 2015) at **Microsoft India (R&D) Pvt. Ltd.**, Hyderabad, in Visual Studio Online Services (Cloud Load Testing team) (using C#, TypeScript, SQL, Java). Have significant contribution towards making the service scalable to support higher configuration and collaboration with another open source load testing tool.
- Worked as **Junior Research Fellow** (Sept 2010 - Jun 2011) in the research project *Virtual Lab for Computer Organization and Architecture*, sponsored by MHRD, Computer Science & Engineering Department, IIT Kharagpur.

Publications

1. *Communicated paper:* **Devleena Ghosh**, Chittaranjan Mandal; "Clustering Based Parameter Estimation of Thyroid Hormone Pathway"
2. Gargi Roy, **Devleena Ghosh**, Chittaranjan Mandal; "COLDVL: a virtual laboratory tool with novel features to support learning in logic design and computer organisation", *Journal of Computers in Education (2017).* doi:10.1007/s40692-017-0091-8
3. **Devleena Ghosh**, Chittaranjan Mandal; "Layout Validation using Graph Grammar and Generation of Yard Specific Safety Properties for Railway Interlocking Verification" in *22nd Asia Pacific Software Engineering Conference (APSEC)* 2015, New Delhi, December, 2015. http://ieeexplore.ieee.org/abstract/document/7467318/.
4. Gargi Roy, **Devleena Ghosh**, Chittaranjan Mandal; "A Virtual Laboratory Package to Support Teaching of Logic Design and Computer Organization" in *7th IEEE International Conference on Technology for Education (T4E)* at NIT Warangal, India, December, 2015. http://ieeexplore.ieee.org/abstract/document/7395606/
5. Gargi Roy, **Devleena Ghosh**, Chittaranjan Mandal, Indraneel Mitra; "Aiding Teaching of Logic Design and Computer Organization Through Dynamic Problem Generation and Automatic Checker Using COLDVL Tool" in *7th IEEE International Conference on Technology for Education* at NIT Warangal, India, December, 2015. http://ieeexplore.ieee.org/abstract/document/7395608/