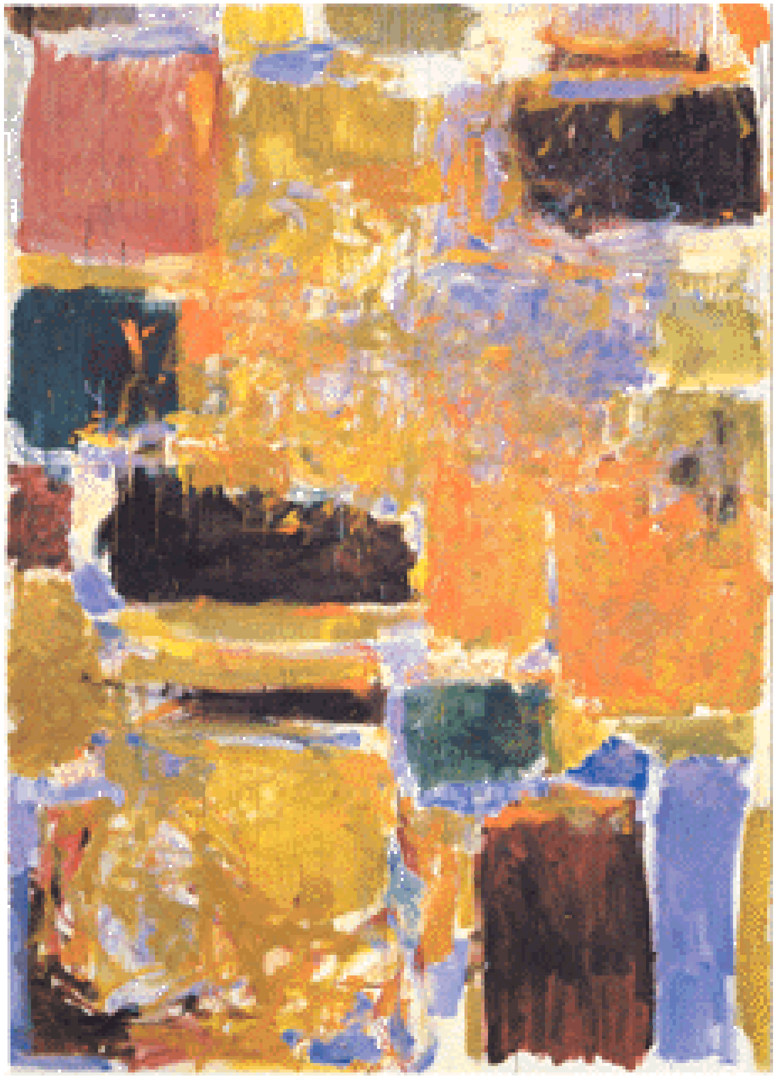


CAD for VLSI

Debdeep Mukhopadhyay
IIT Madras

Tentative Syllabus

- Overall perspective of VLSI Design
- MOS switch and CMOS, MOS based logic design, the CMOS logic styles, Pass Transistors
- Introduction to Verilog HDL
- Combinational logic Design: Simplification of switching functions, K-map based reductions of switching circuits, complex designs using multiplexers/demultiplexers, decoders
- PLAs and their use in standard combinational logic design.

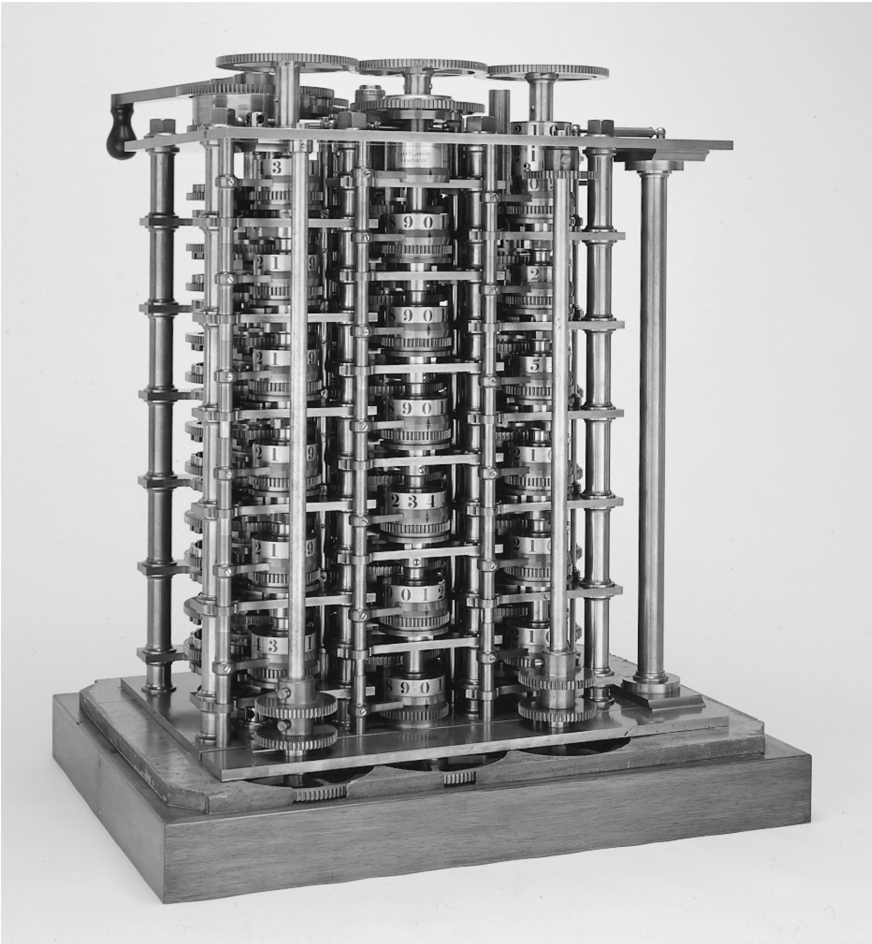
Tentative Syllabus

- Memory elements: flip-flops, latches, registers.
- Sequential logic Design: Concepts and state diagrams.
- VLSI Design Issues:
  - Timing in Digital Circuits
  - Power Issues
  - and Parasitics
- Data Path Design: Realizations of Computational blocks, like adders, multipliers, CORDIC

Laboratory Work

- This is an Engineering Course. So, we shall have assignments and lab works integrated with this course. Please be sincere about them.
- Assignments shall encompass:
  - Verilog Coding
  - Developing knowledge of Standard CAD flow
    - ASIC Flow
    - FPGA Flow

The First Computer

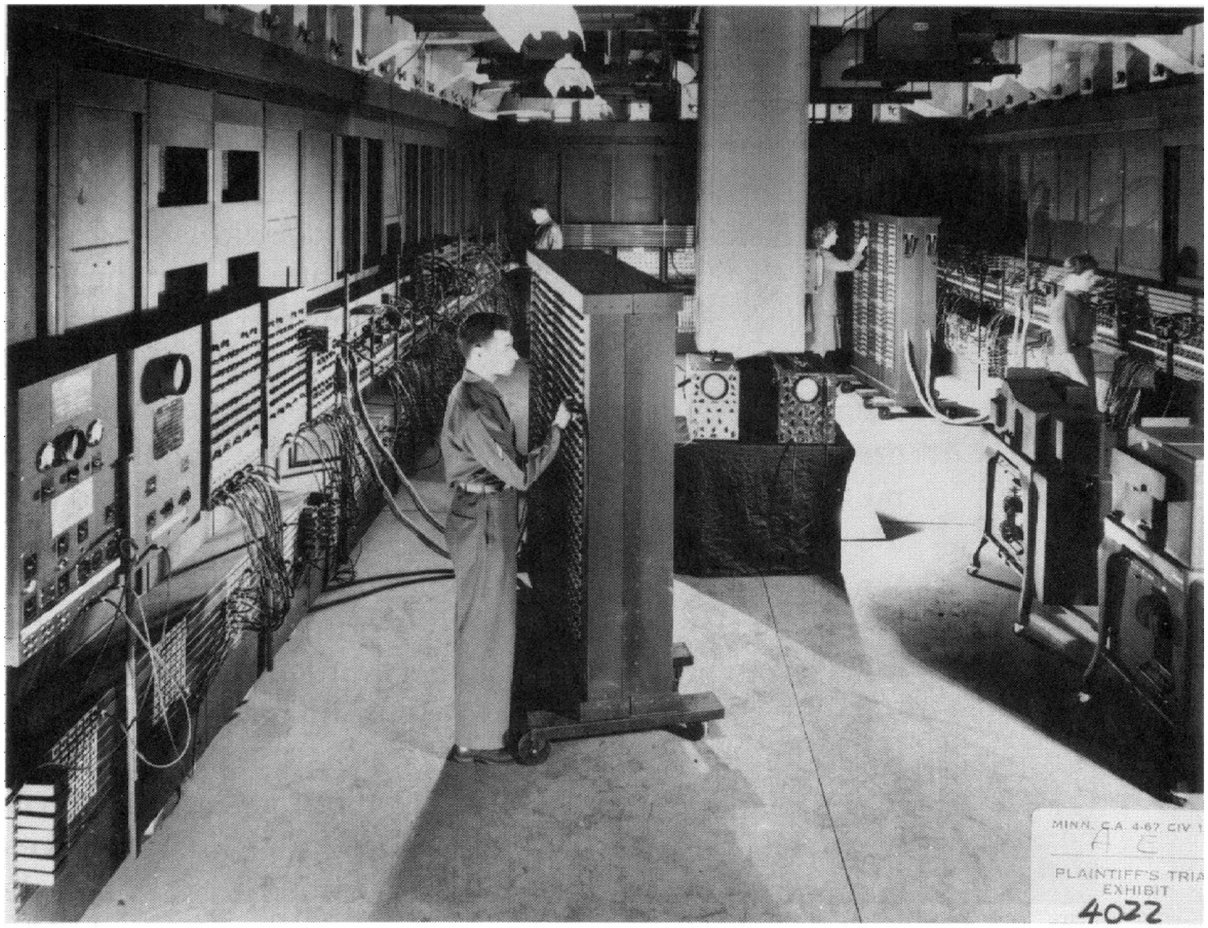


The Babbage Difference Engine (1832)

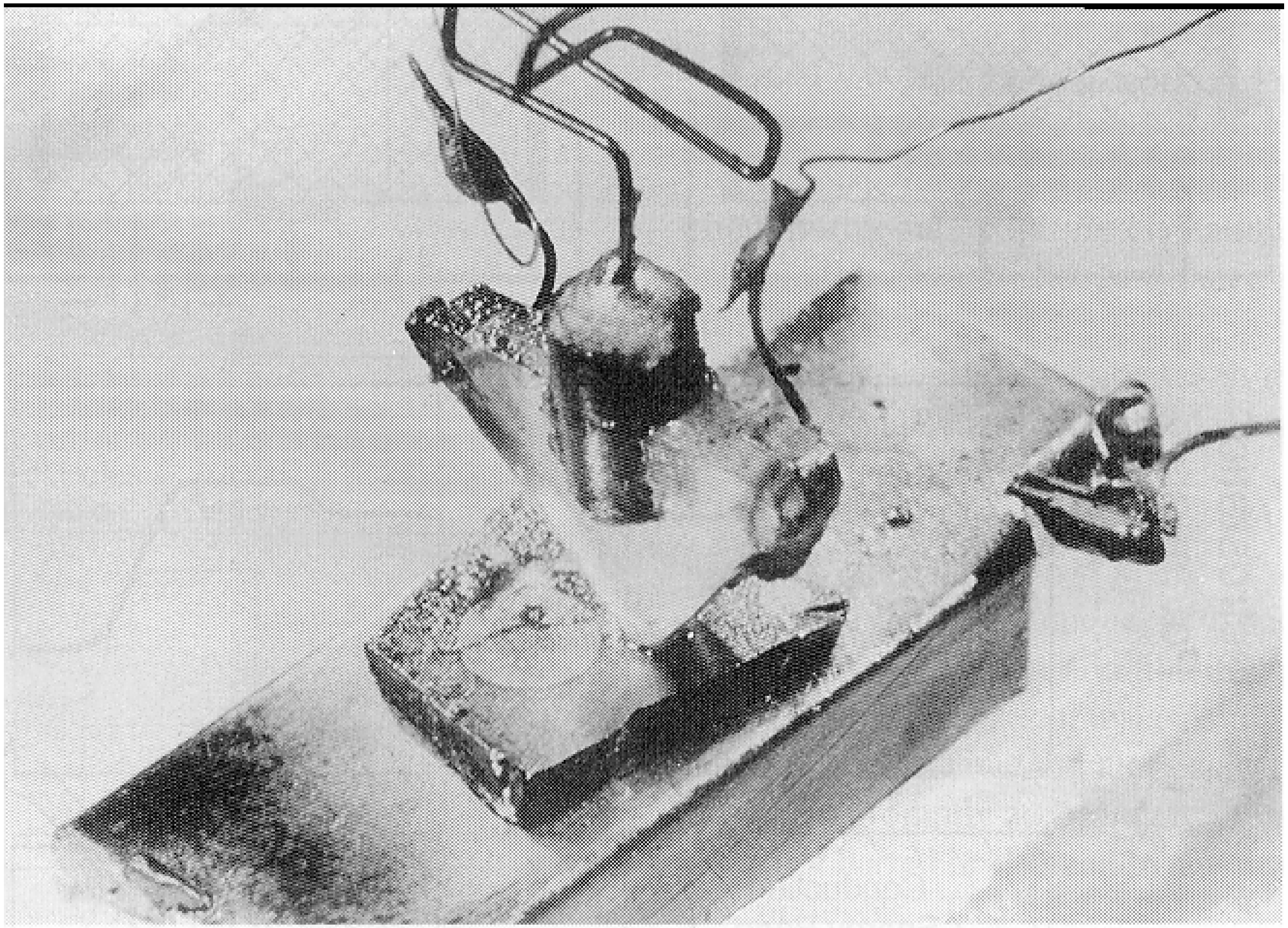
25,000 parts

cost: £17,470

ENIAC - The first electronic computer (1946)

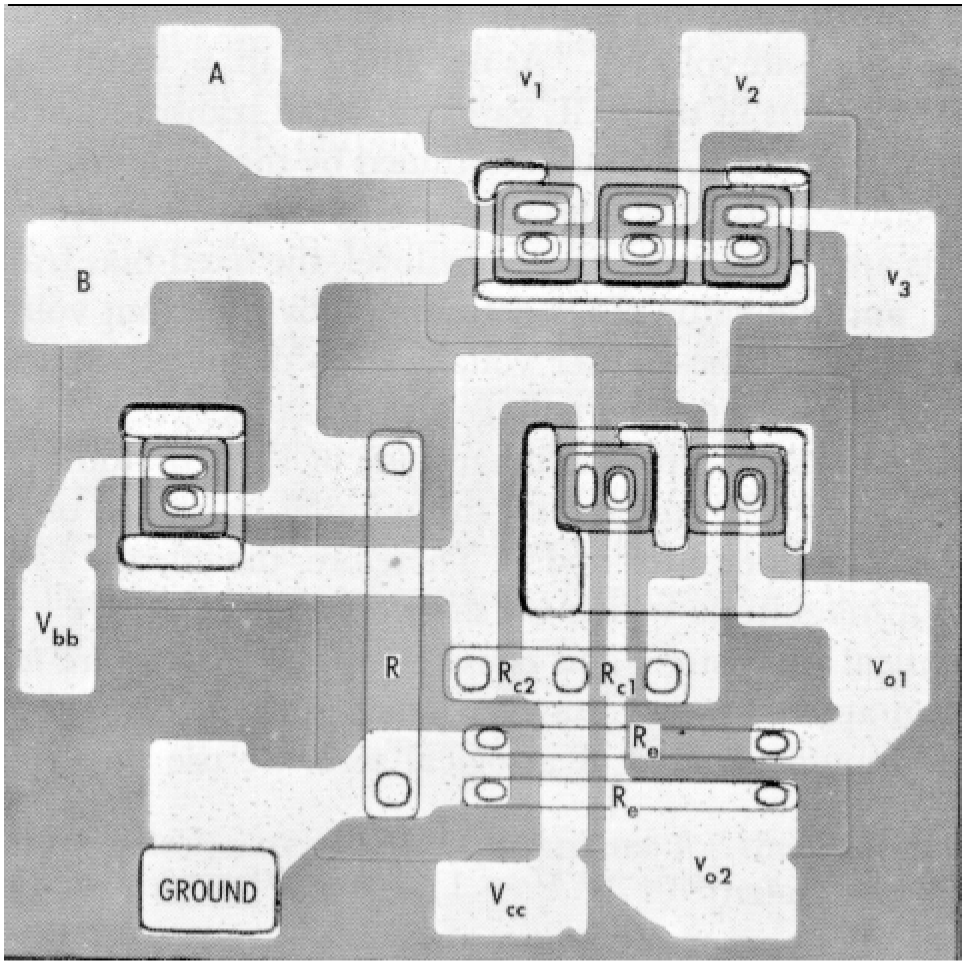


The Transistor Revolution



First transistor
Bell Labs, 1948

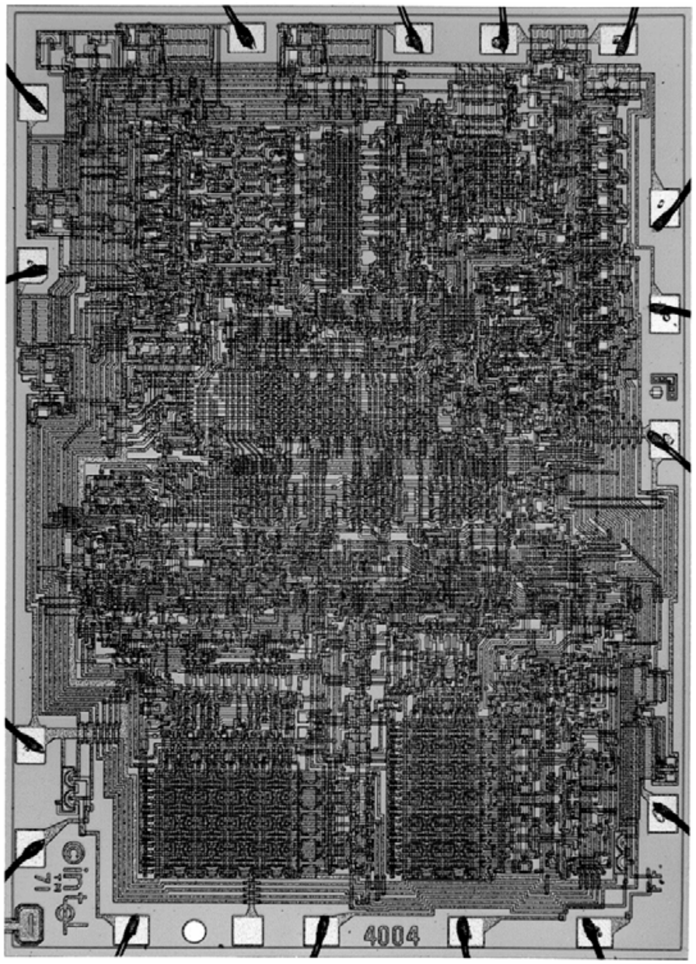
The First Integrated Circuits



Bipolar logic
1960's

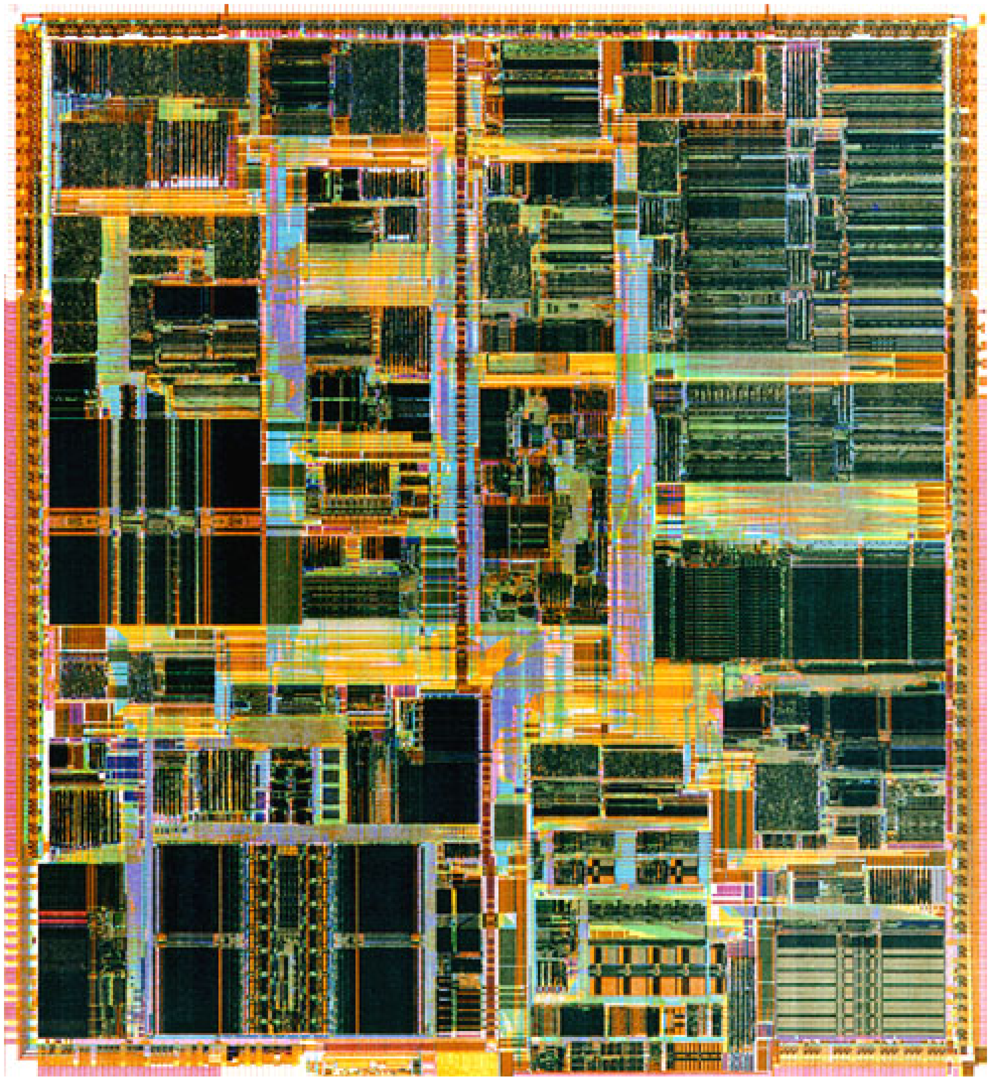
ECL 3-input Gate
Motorola 1966

Intel 4004 Micro-Processor



1971
1000 transistors
1 MHz operation

Intel Pentium (IV) microprocessor



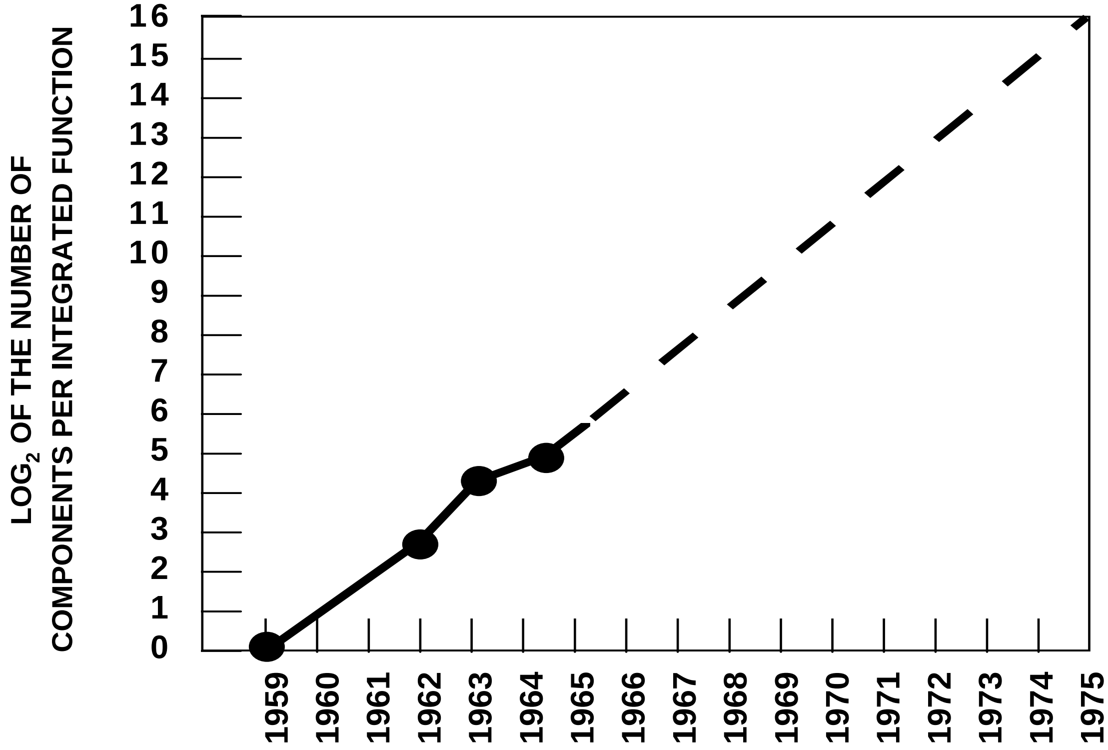
Computer-Aided Design

- 1967: Fairchild develops the "Micromosaic" IC using CAD
- 1968: Noyce, Moore leave Fairchild, start Intel

Moore’s Law

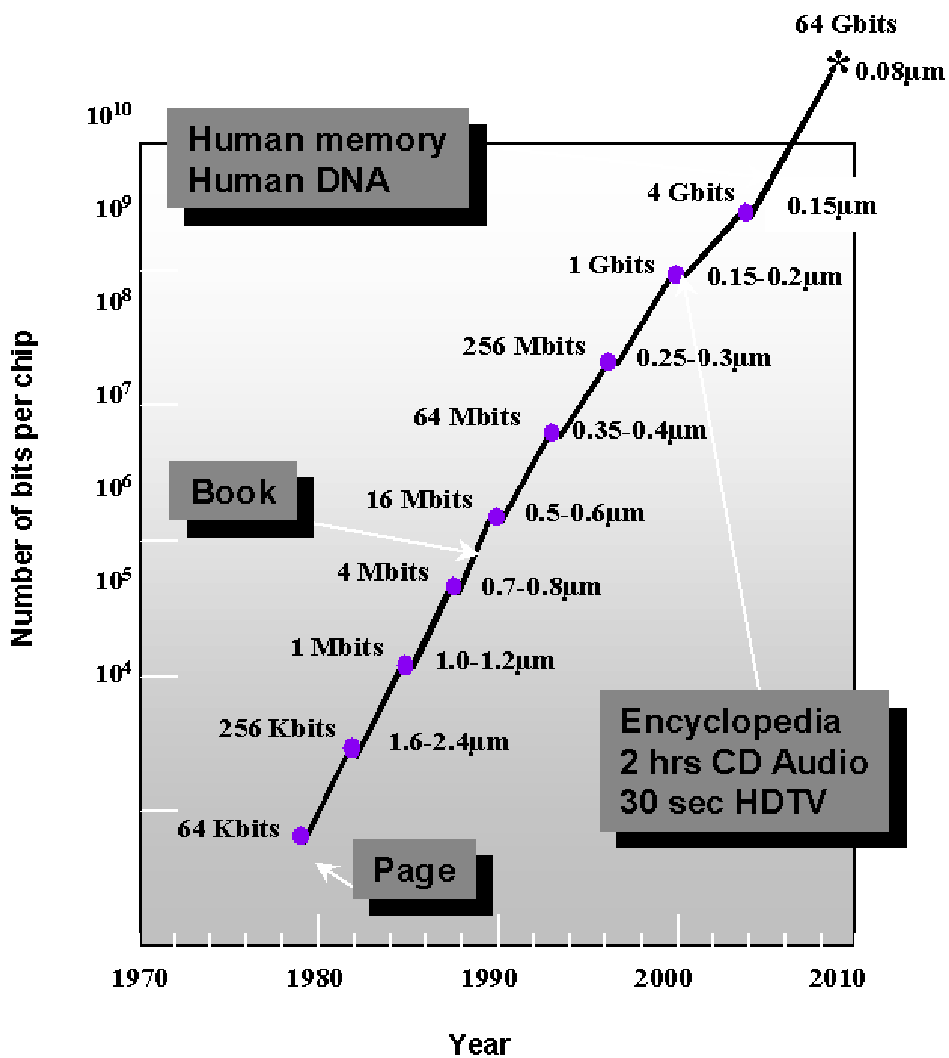
- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

Moore's Law

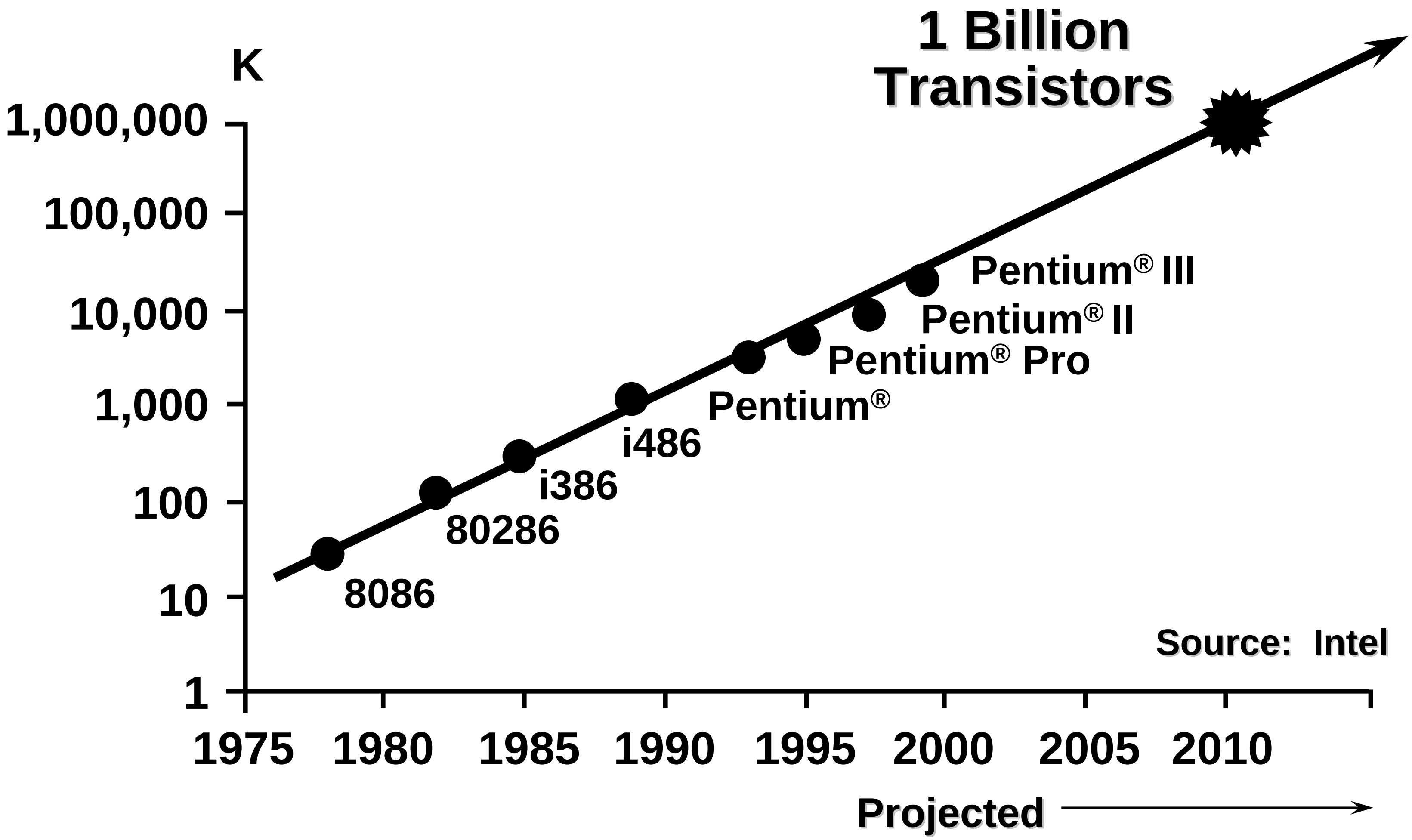


Electronics, April 19, 1965.

Evolution in Complexity



Transistor Counts

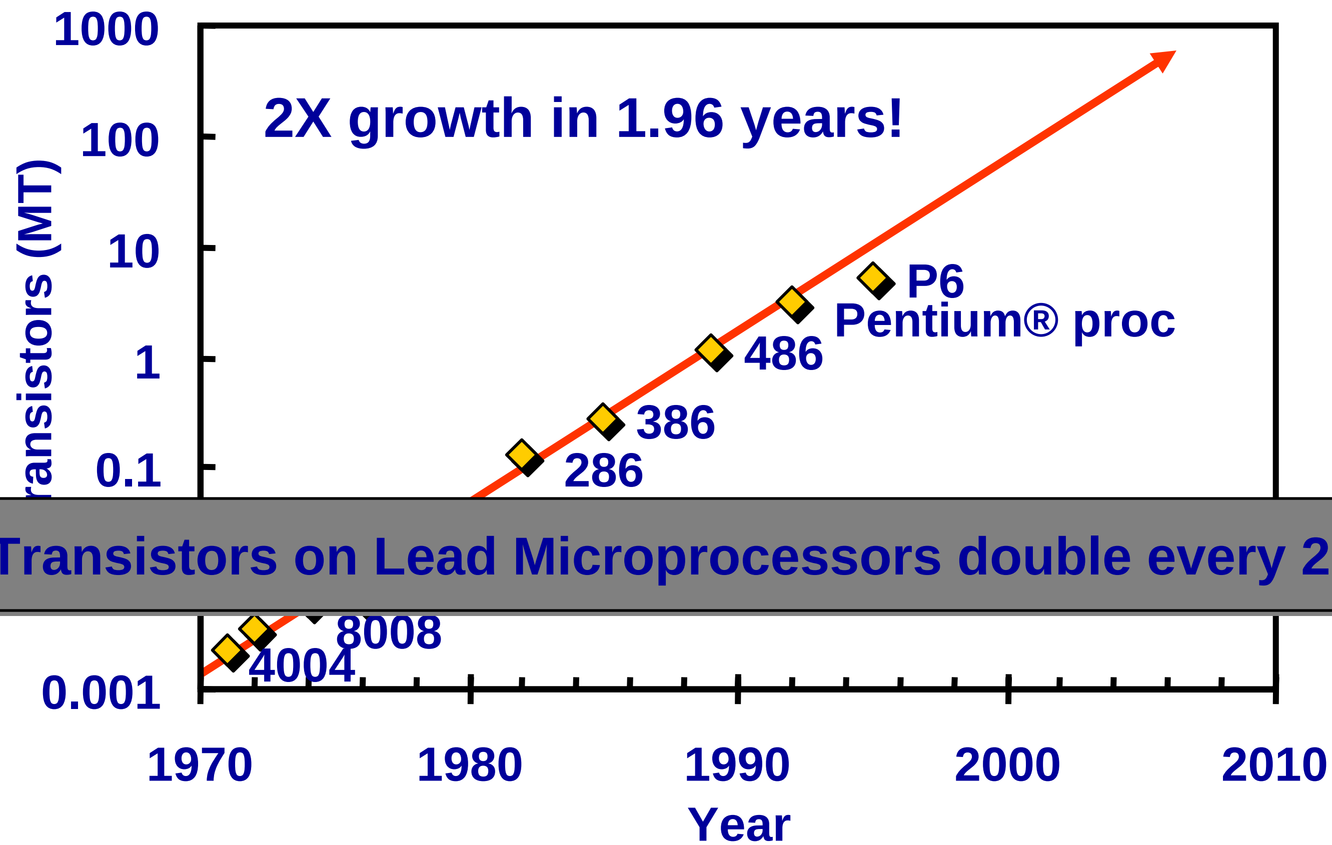


Courtesy, Intel

Evolution of Micro-electronics

Year	1947->	1950->	1961->	1966->	1971->	1980->	1990->	2000->
No of trans Per chip	1	1	10	100-1000	1000-20,000	20,000-1 M	1 M-10M	>10M
Typical product	-	Junction Transistor	Planar Devices, Logic gates, FFs	Counters, mux, adders	8 bit uP, ROM, RAM	16 bit uP, DRAM	Special processors, virtual reality m/cs	
Technology	Transi-stor	Discrete Components	SSI	MSI	LSI	VLSI	ULSI	GSI

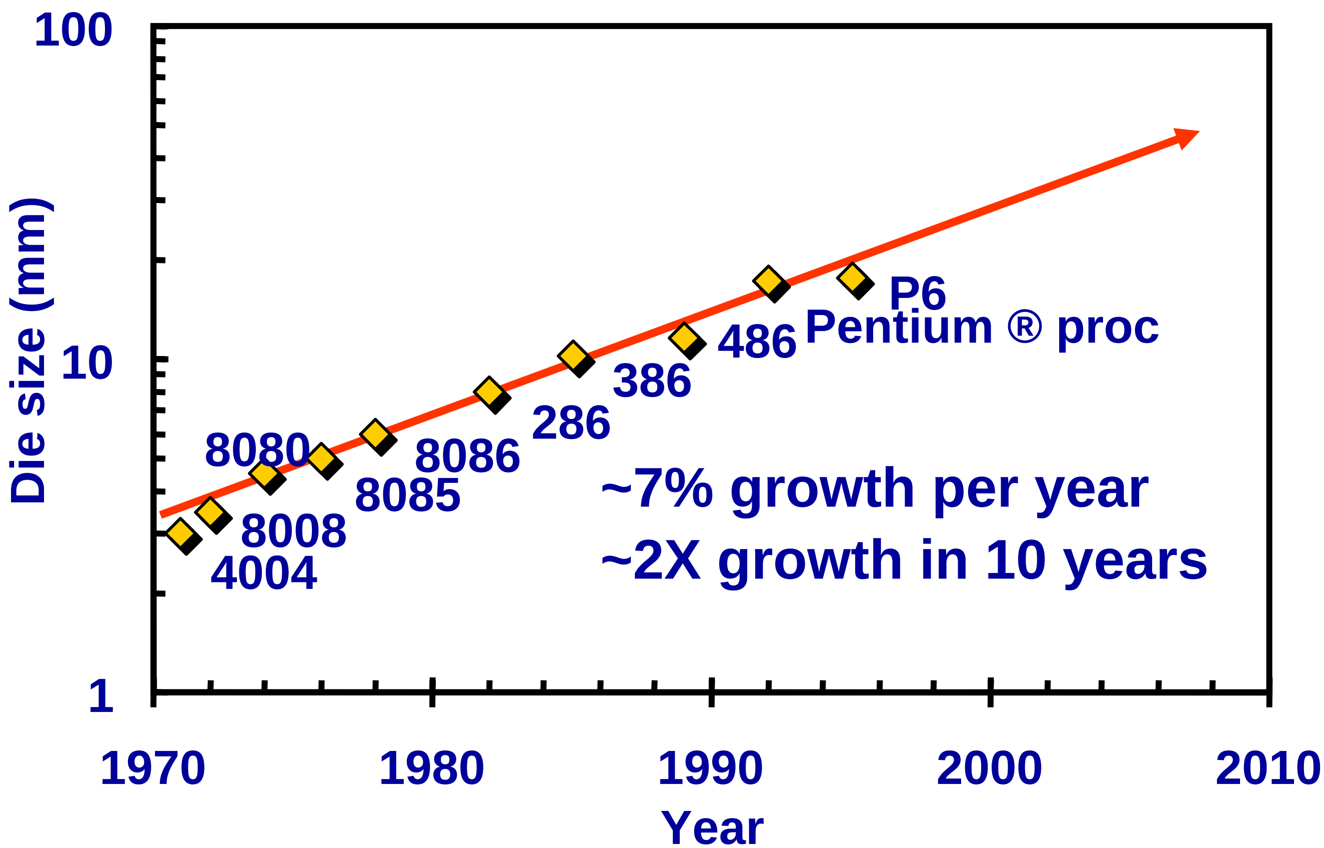
Moore's law in Microprocessors



Transistors on Lead Microprocessors double every 2 years

Courtesy, Intel

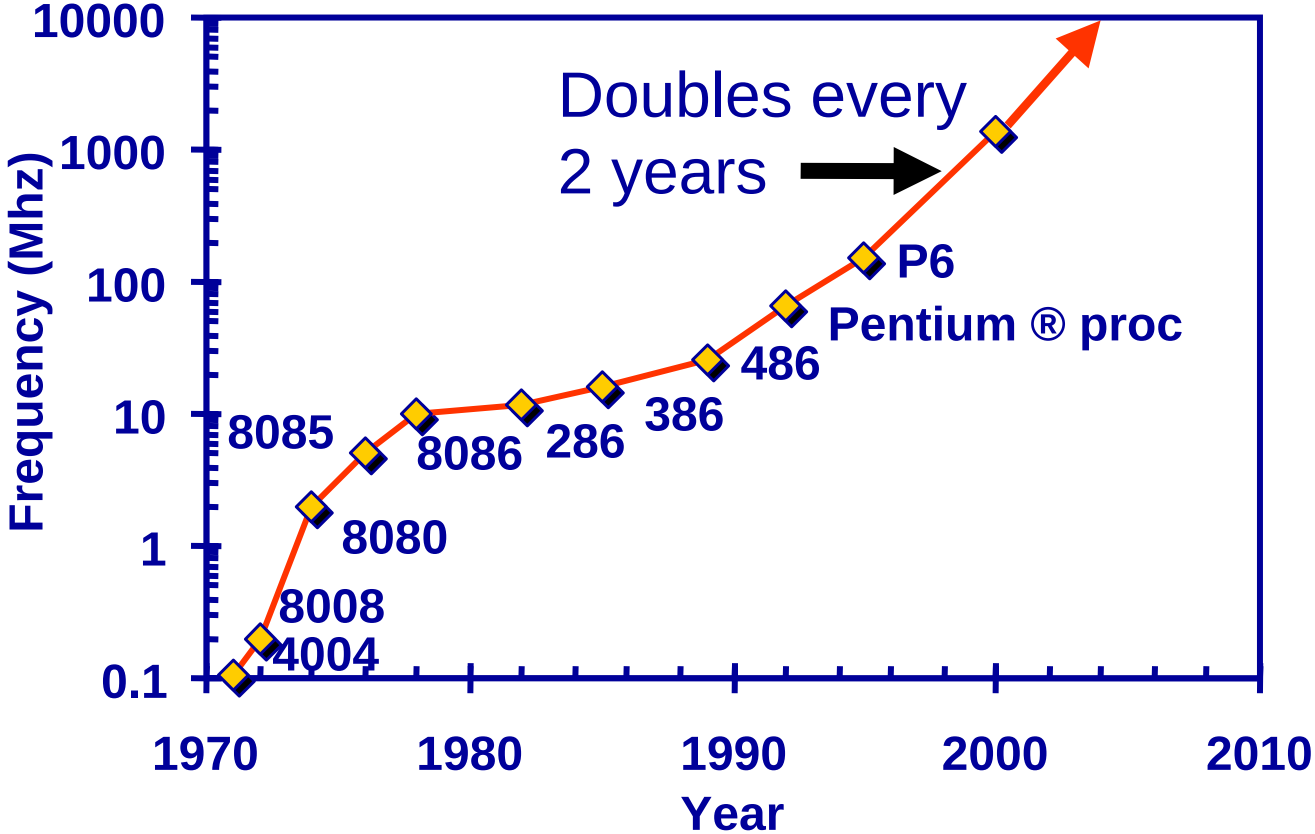
Die Size Growth



Die size grows by 14% to satisfy Moore's Law

Courtesy, Intel

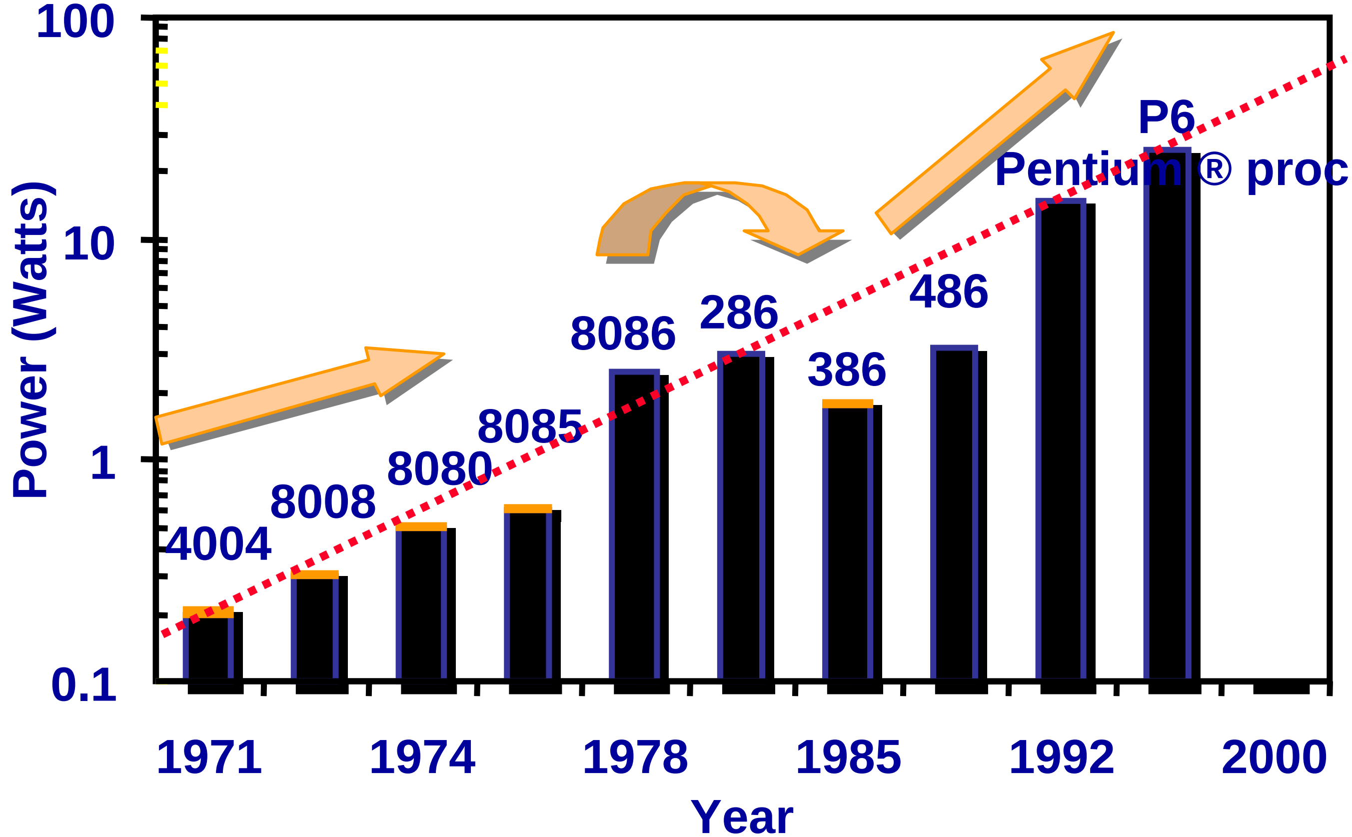
Frequency



Lead Microprocessors frequency doubles every 2 years

Courtesy, Intel

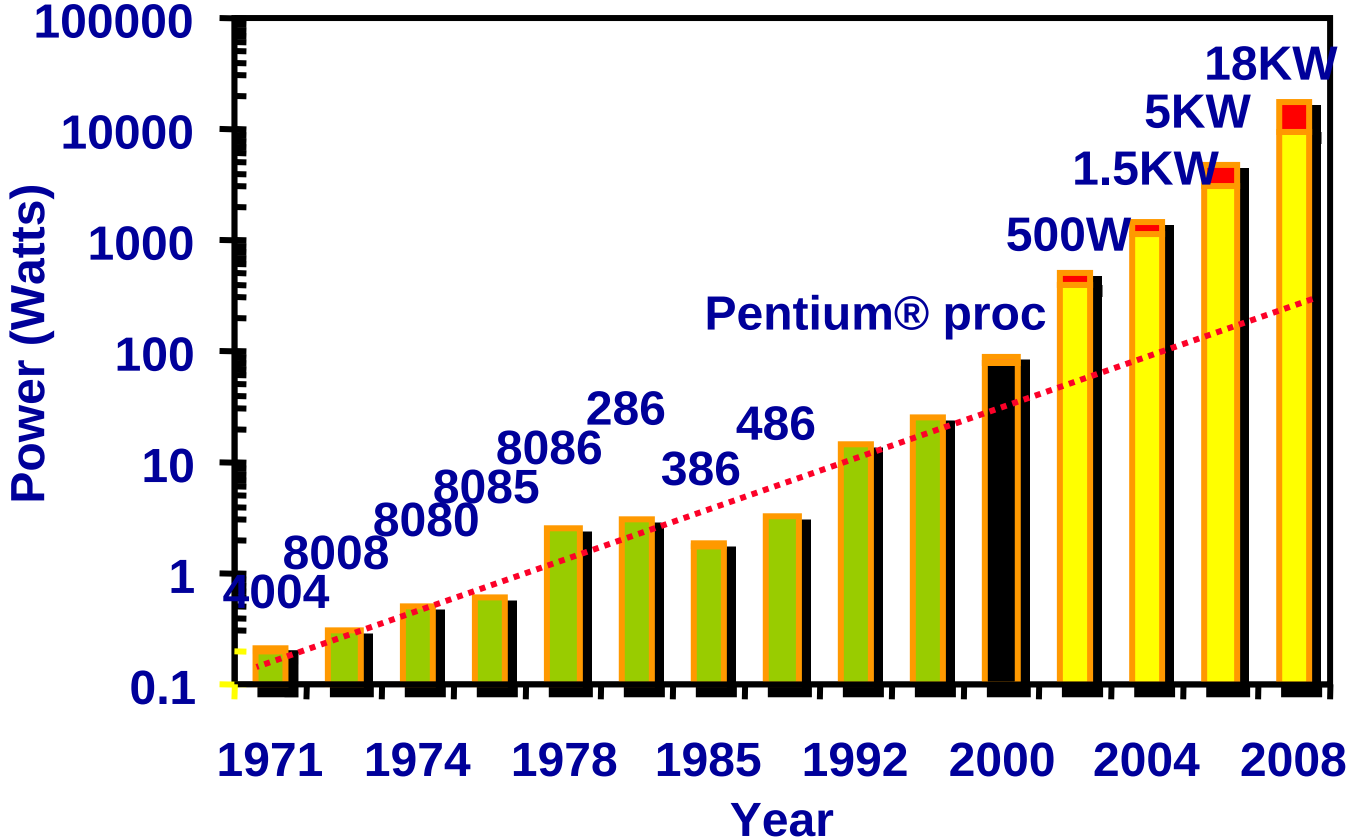
Power Dissipation



Lead Microprocessors power continues to increase

Courtesy, Intel

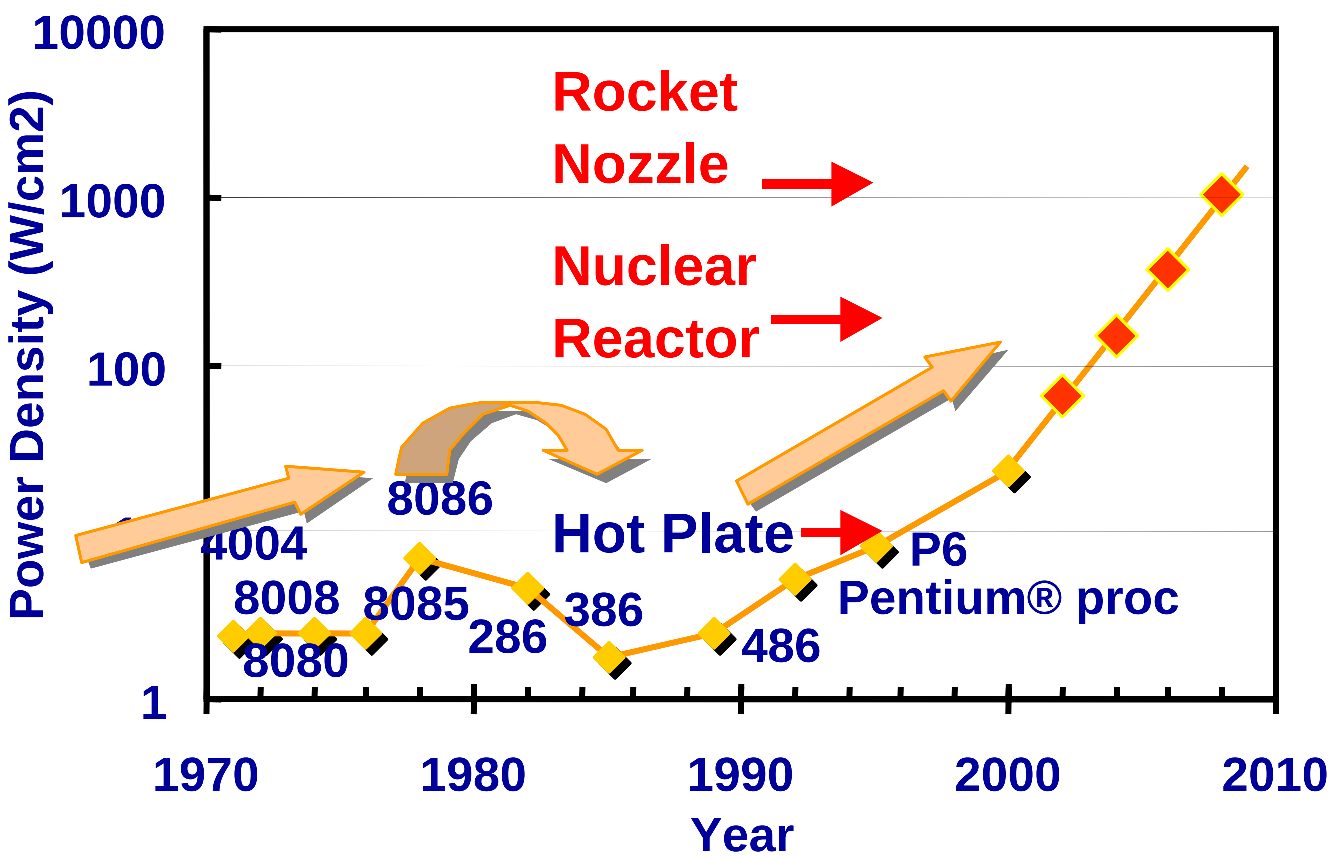
Power will be a major problem



Power delivery and dissipation will be prohibitive

Courtesy, Intel

Power density



Power density too high to keep junctions at low temp

Courtesy, Intel

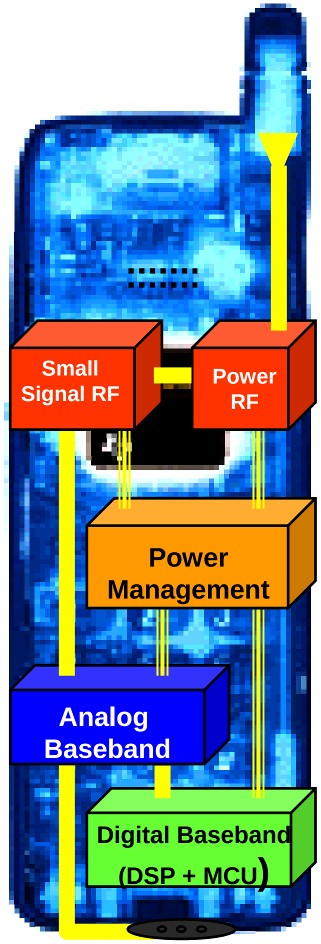
Not Only Microprocessors

Cell
Phone

Digital Cellular Market
(Phones Shipped)

	1996	1997	1998	1999	2000
Units	48M	86M	162M	260M	435M

(data from Texas Instruments)



Challenges in Digital Design

∝ DSM

"Microscopic Problems"

- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

Everything Looks a Little Different

?

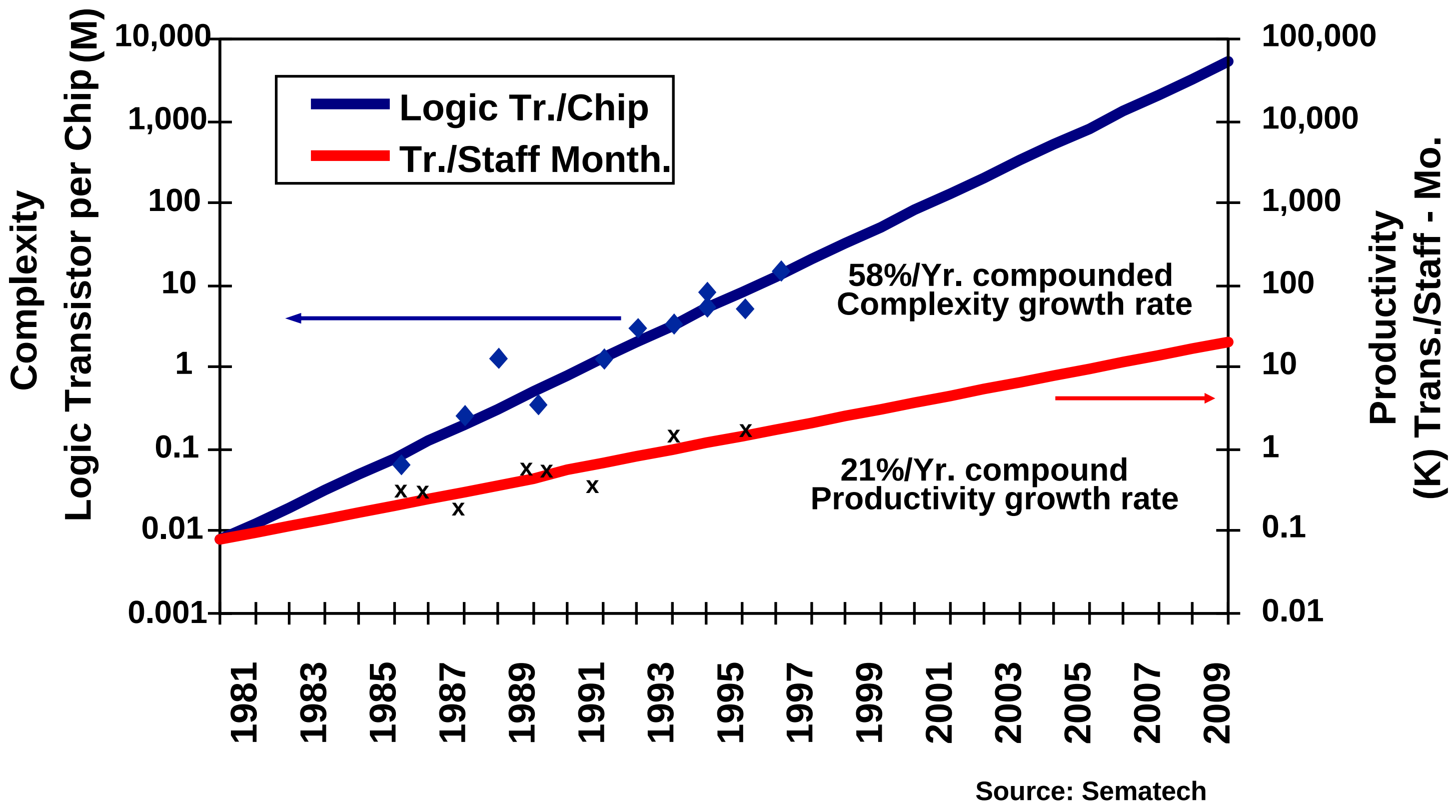
∝ 1/DSM

"Macroscopic Issues"

- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- etc.

…and There's a Lot of Them!

Productivity Trends



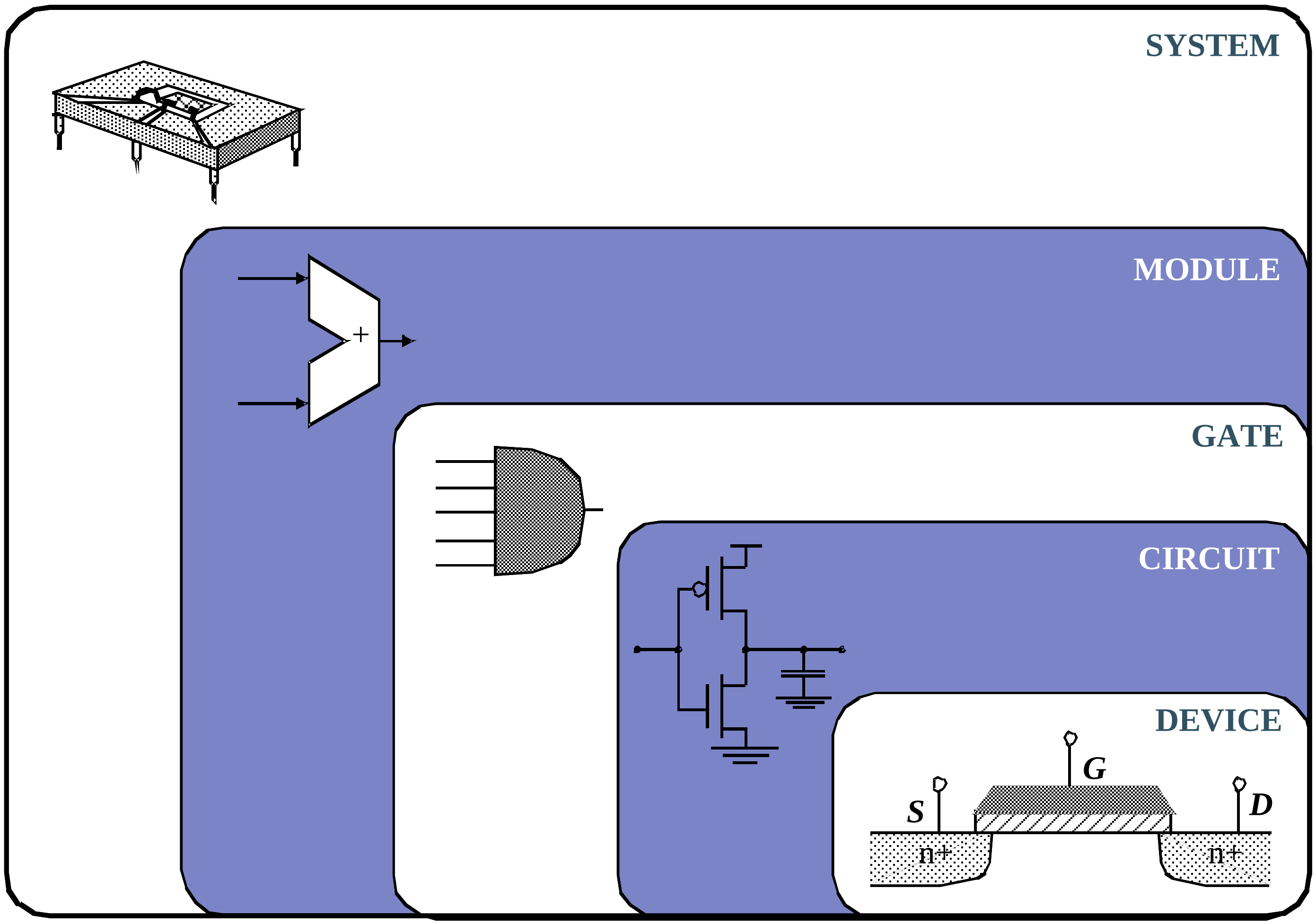
Complexity outpaces design productivity

Courtesy, ITRS Roadmap

Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Design Abstraction Levels



But Reality is complex!

- Advancement of technology requires designing and implementing module libraries.
- Require to understand critical paths of design to evaluate its performance.
- Library based design is fine for Application specific designs. But not so for high performance designs: Full custom…

But Reality is complex!

- Interconnect parasitics: capacitances, resistances and inductances.
- Clock distribution and power supply distribution.
- Power constraint as a design issue.
- Murphy's law : "Whatever can go wrong, will go wrong“. So, troubleshooting has to be learnt.

Examples

- Clocks Defy Hierarchy
  - Why do we require clocks?
  - Clock Skews.
  - Effect of clock skews on a hierarchically designed system
- Power dissipation networks defy hierarchy:
  - planning a power distribution requires estimation of loading, direction of current, information about total peak power drawn from the supply etc…
  - have to defy the boundaries of hierarchical design, plan dedicated area for the power network.

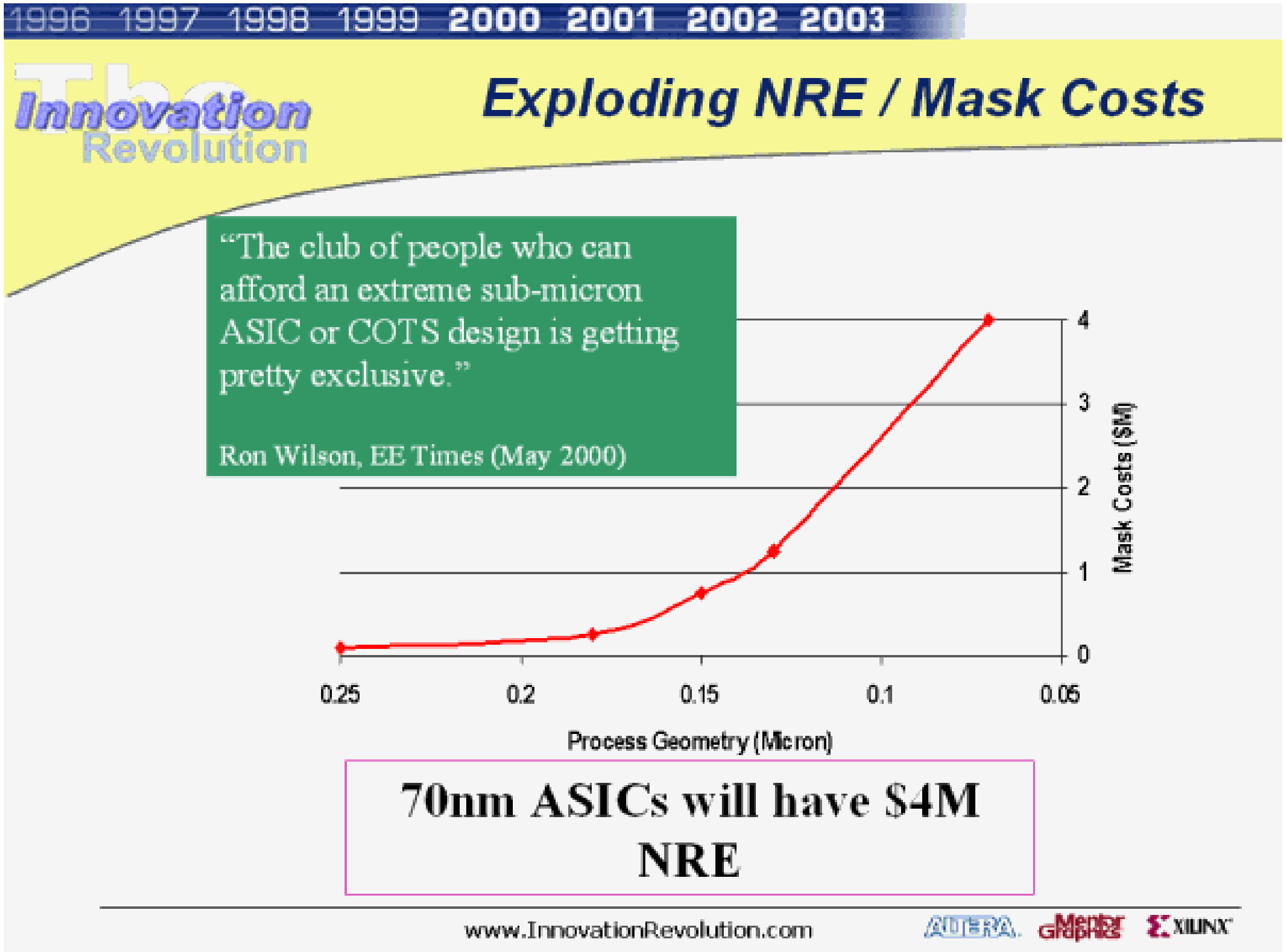
Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

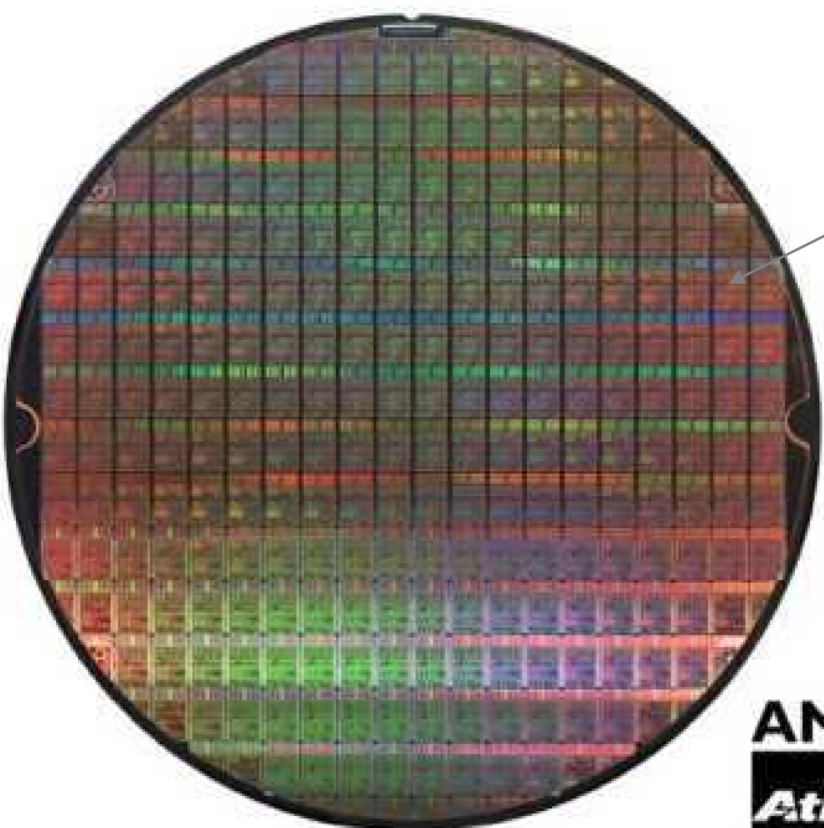
Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs
  - cost of work done by ASIC vendor, mask generation
  - \$10,000-\$3,00,000 (Mask cost: \$5000-\$50,000)
  - production test cost
- Recurrent costs
  - silicon processing, packaging, test
  - proportional to volume
  - proportional to chip area

NRE Cost is Increasing



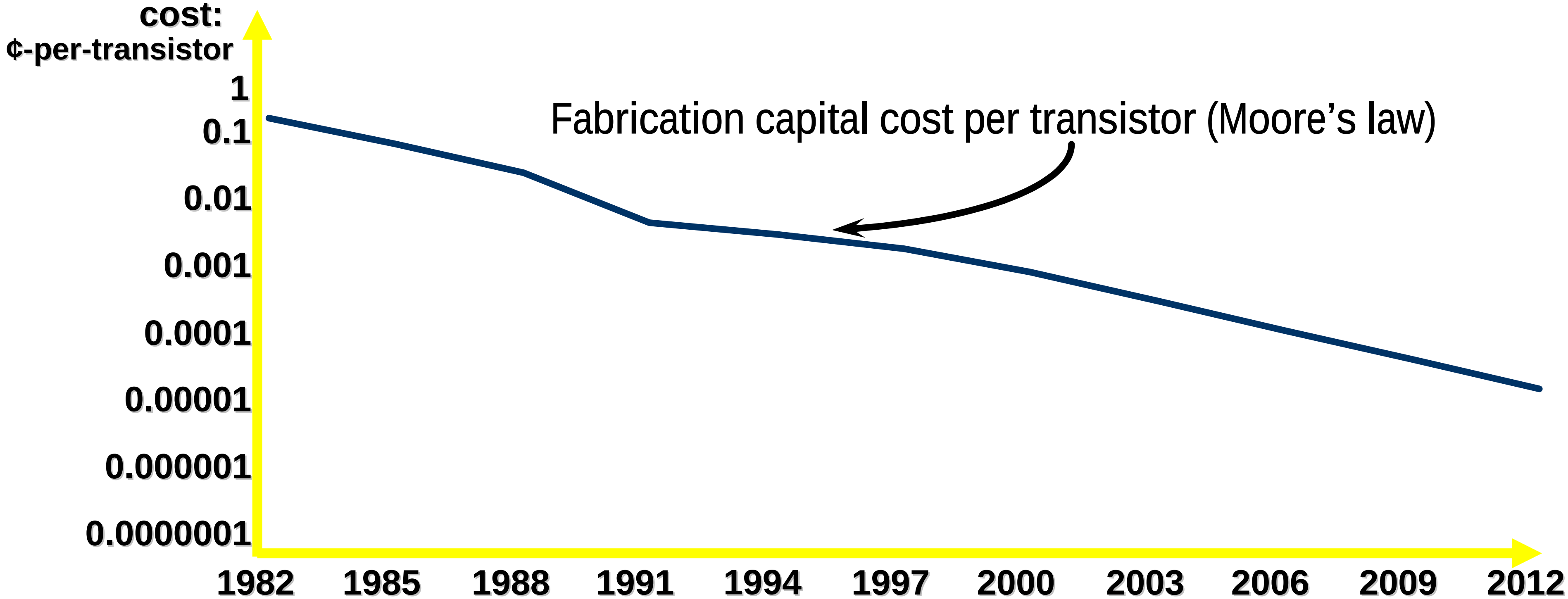
Die Cost



Going up to 12” (30cm)

From http://www.amd.com

Cost per Transistor

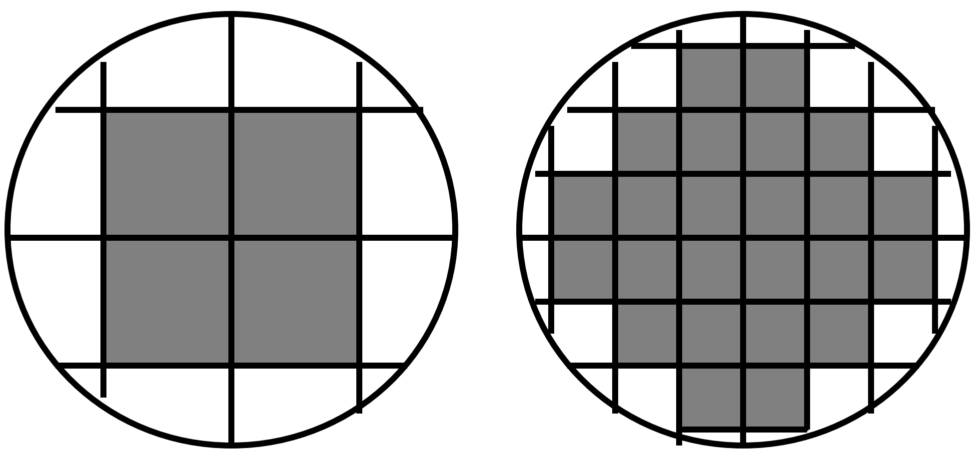


Yield

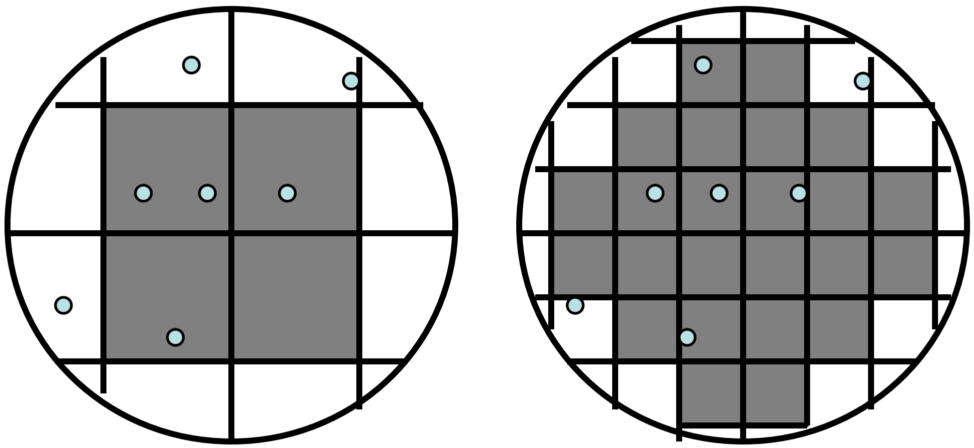
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$



Defects



$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

α is approximately 3

$$\text{die cost} = f\,(\text{die area})^4$$