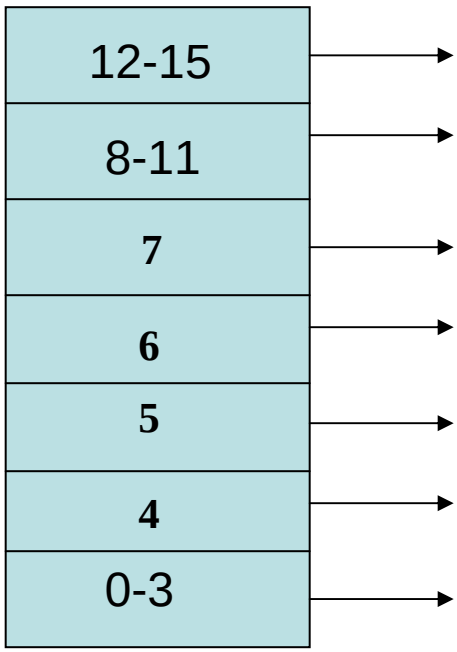
Assignment 1

- **<u>Problem 1:</u> Write a verilog code for a four bit address decoder. It provides enable signals for segments of memory, the address map of which is shown below.**



- **<u>Problem 2:</u>**

Design a generic n-bit input, m-bit output binary decoder, with a separate enable input.

Instantiate the written module from another module, to realize a (2,4) and (3,6) decoder.

- **<u>Problem 3:</u> Compare the if else, nested if, case and for coding styles for modeling of various combinational blocks in terms of simulation time, cpu utilization and memory utilization of the processor. You can add any other interesting metric of your choice.**