RTL and Gate Level Power Analysis Flow with Synopsis Tools

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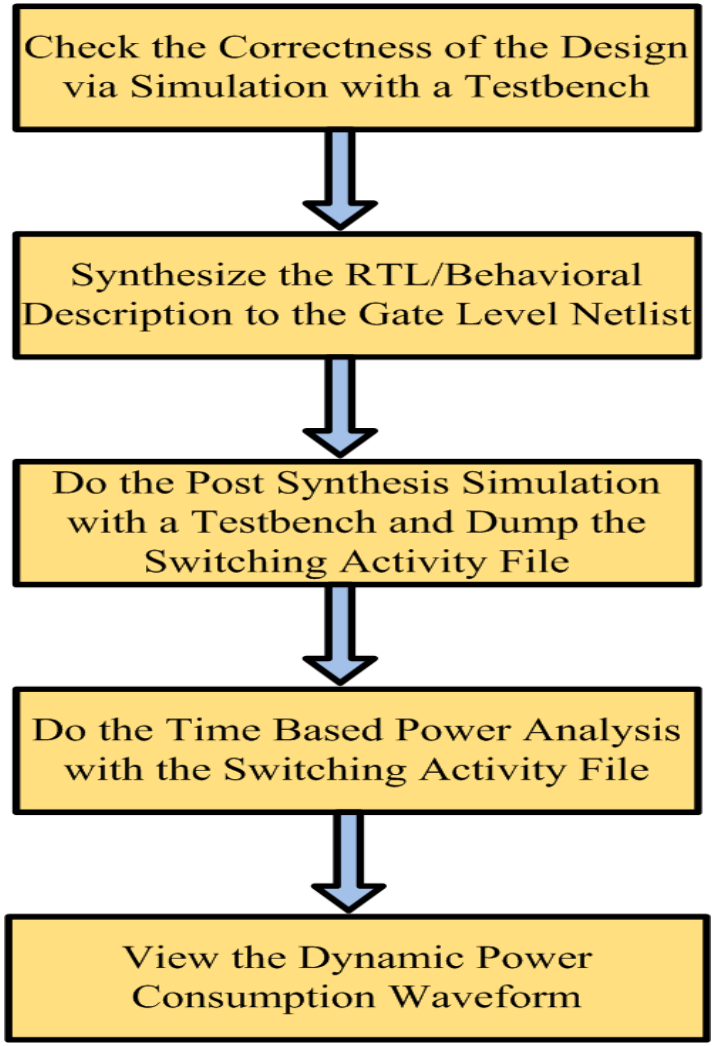
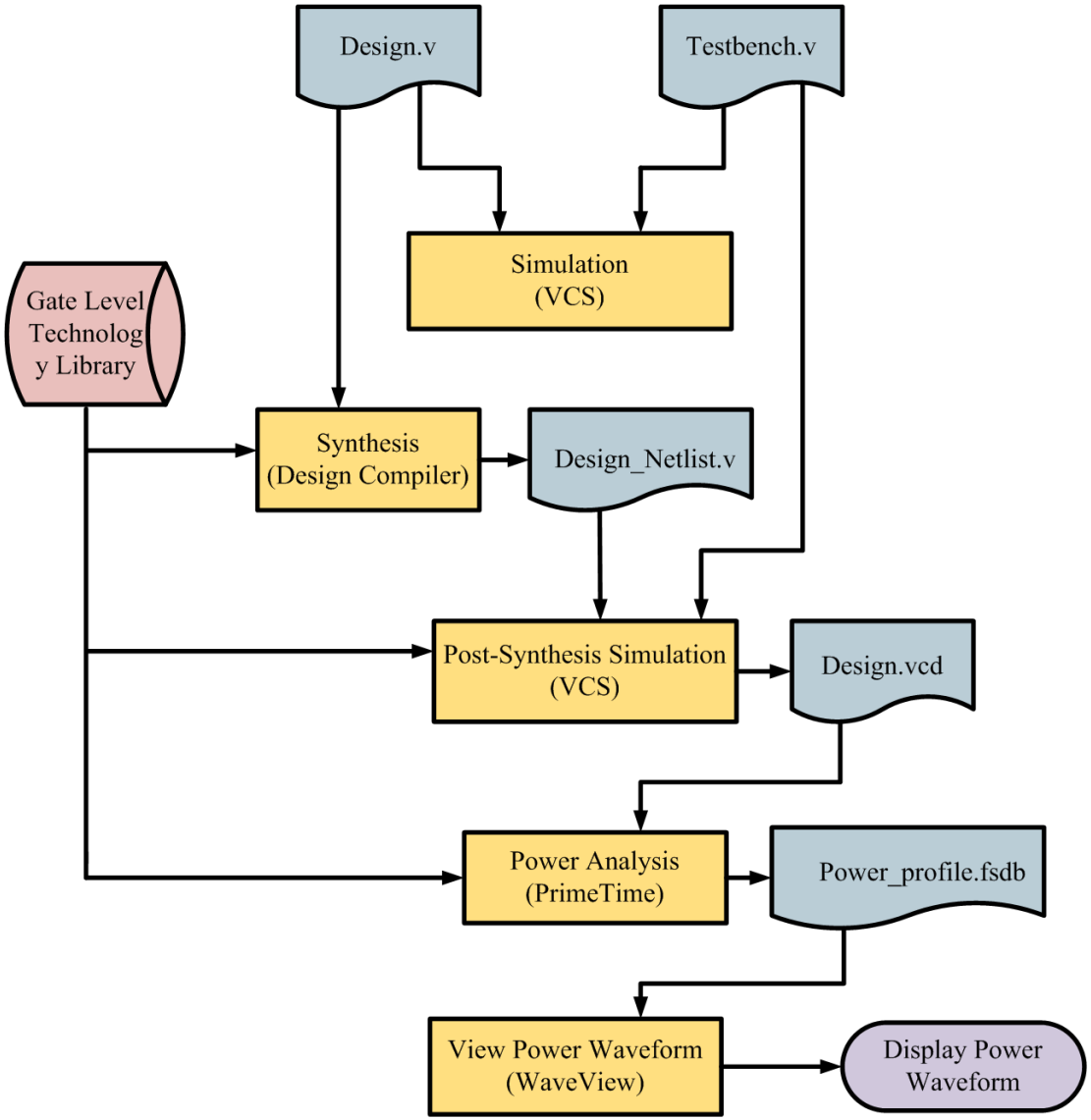
Technology Used

- Tools:
  - Synopsys VCS Simulator.
  - Synopsys Design Compiler.
  - Synopsys PrimeTime.
  - WaveView

Basic Flow


Check the Correctness of the Design via Simulation with a Testbench
Synthesize the RTL/Behavioral Description to the Gate Level Netlist
Do the Post Synthesis Simulation with a Testbench and Dump the Switching Activity File
Do the Time Based Power Analysis with the Switching Activity File
View the Dynamic Power Consumption Waveform

Detailed Flow



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Example Waveform: Composite Field AES Implementation

- Input Files:
  - Composite field implementation of AES in Verilog.
  - Testbench in Verilog.