BUS FUNCTIONAL MODELS:
WRITING TRANSACTION LEVEL TEST-BENCHES

1. Write a verilog file to model a memory: Declare a two dimensional array mem, using the following statement:

reg [M-1:0] mem [N-1:0];

Use the address to field to either read from or write onto a memory address location, depending on the value of the ~READ or ~WR signals.

Hint: Declare data as inout and address as input.

2. Write verilog tasks (BFMs) for the read and write operations. The timing specifications are as follows:

READ: Select the memory by lowering a CS signal. Latch the address, after 3ns (enable) lower the READ signal, hold the READ signal low for 5ns (so that the read data is stable)

WRITE: Select the memory by selecting a CS signal. Signal WE must wait for 3 ns after the address is stable, after which the WE signal is lowered (enabled). The WE signal is held low for a time of 5ns after the data is stable.

3. Write an 'e' routine to write and read to and from the memory.

4. Think of extending this to a multiple memory architecture.