Digital Design Verification (CS 676)
Dept of Computer Sc and Engg, IIT Madras
Mid Semester Examination
Answer all Questions *Time: 2.5 hours*
Full Marks: 25

1. What is the full form of HVLs and why are they important in the VLSI industry? Explain in short.

(2 marks)

2. Write a short note on the following terms bringing out the difference between the two:

a. Formal and assertion based verification
b. Random and Directed verification

(3 marks)

3. Dual port RAM (DPRAM) provides a common memory accessible to 2 processors that can be used to share and transmit data and system status between two processors.

Consider a DPRAM wrapper in verilog:

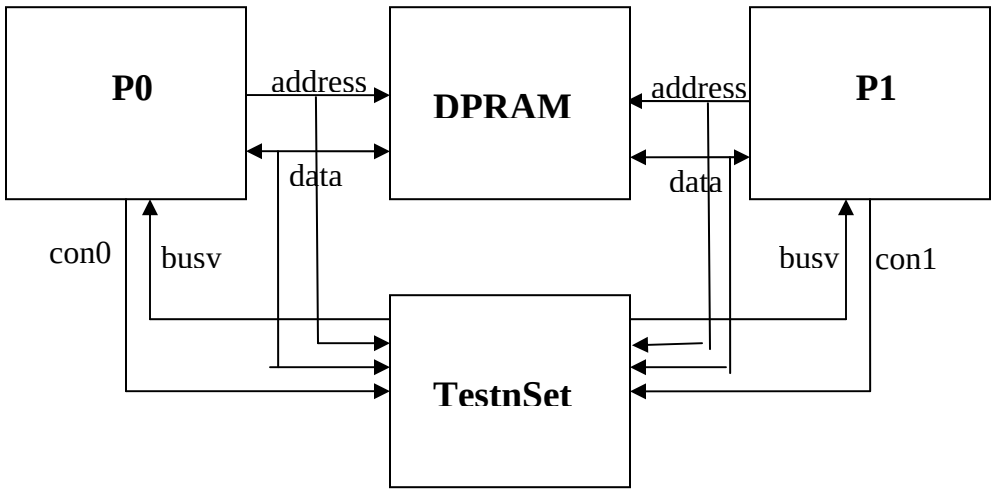
dram(addr0, data0, addr1, data1)

The dimension of the data bus is 1 bit and that of the address bus is 4 bits. The wrappers, written in verilog has tasks **read_memory** and **write_memory** which you can invoke from a top level test-bench.

We also have suitable wrappers for the verilog codes for a processor:

cpu(busy,addr,data,control)

The control and busy bits are 1 bit each and the data and address are as that of the DPRAM.



A block named TestnSet probes two processors P0 and P1 which share a DPRAM. The processors are connected to port0 and port1 of a shared DPRAM (refer Fig). The block named TestnSet maintains two special 1 bit registers sreg0 and sreg1 and two 1 bit flag registers, flag0 and flag1.

If the control bit of P0 goes high with the address value as say A, then the content of the memory is brought to the sreg0 and flag0 is set high. If P1's control bit also goes high and address value is also A, then P1 busy should be high. Otherwise there is an error. Irrespective of what happens to P1, the sreg0 register will be checked and if the value is 0, the content of data0 bus will be written to the address A. If the sreg0 register is 1, no write takes place.

Write an e code to verify the block TestnSet. Access the necessary verilog codes using the wrappers provided.

Please state any assumptions that you have made.

(10 marks)

4. A communication device receives a clock upto M MHz. Write a verilog code snippet to verify that the clock meets this timing requirement.

(Hint: Use fork and join constructs)

(5 marks)

5. Comment briefly on the following:

a) 100% functional coverage ensures that the design can have no bugs.

b) 100% code coverage guarantees that the test bench is very well written.

(3+2=5 marks)