Quiz-2
DIGITAL DESIGN VERIFICATION (CS: 676)

Answer all questions **Time: 1hr**
Full Marks 15
Dt: 13/4/2007

1. Write an e-code snippet to verify the following assertion regarding the exchange between Block1 and Block2. The request may be asynchronous.
If req goes high, ack goes high 3 clocks later, which causes req to go low 7 clock cycles later. (5 marks)

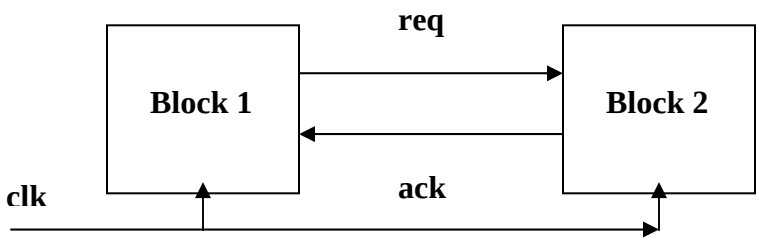

Fig. 1

2. Packets dispatched can be of 3 network types: atm, ieee or Ethernet. The packets have a Boolean flag field which indicates whether the packet is "good" or "bad". The header of the packets is 32 bits in length. When the packet is atm, the entire header is randomly generated, but when it is ieee or Ethernet the lowest 4 bits are always zero. 20% of the time atm packets are generated, while remaining time ieee or Ethernet packets are generated uniformly. Model the above scenario using language e.

(5 marks)

3 Write an e code to divide a given clock by 2.

(5 marks)