Transistor Parameter Determination for Digital Circuits

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Transistor Parameter Determination for Digital Circuits

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Abstract

Transistor sizing to achieve desired performance parameters is an important design challenge. Accurate modelling is essential for parameter optimisation. This thesis presents hybrid modelling of CMOS circuits at level 2 and modelling complex CMOS circuits at a higher level i.e. level 49, parameter optimisation and determination of performance parameters (rise time, fall time and power dissipation).

The work in this thesis first models the circuit to be analysed through a set of differential equations based on the behaviour of the transistors and their interconnections. Simple ODE modelling isn't adequate as the transistors may be in various states (cutoff, linear, saturation). Accordingly, a circuit with n transistors may have up to 3^n states. As the circuit operates, it makes transitions between these states (also called locations). ODE modelling is inadequate to capture this kind of situation. To handle this, the modeling of CMOS circuits have been done as a Stateflow model in Matlab Simulink. The standard equations which govern nMOS and pMOS transistors and involve the transistor geometries as parameters have been used.

As a number of locations corresponding to the regions of operations of the transistors are involved, it is important to check that all relevant transitions are adequately covered. This may be called the completeness of the model. In this thesis a mechanism is also presented to determine the completeness of the modelling of the circuit.

In each location, corresponding to the regions of operation of the transistors, Spice Level 2 model equations have been considered which include second-order effects. These equations are directly related to the specification of different parameters of the transistors. To describe different operating regions of the transistors, the differential equations have been formulated. The mechanism has been successfully demonstrated on a CMOS inverter, a CMOS NAND2 and CMOS NOR2 gate. An efficient modeling technique has been developed for CMOS circuits with separate networks of pMOS/nMOS transistors for pull-up/pull-down operations. The output waveform of the Stateflow model is displayed in a display box with respect to the imulation

time. The advantage of the present modeling technique is that Stateflow models are comparable with respect to real circuit simulation results and the model evaluation time is comparatively fast.

The thesis then presents complex CMOS circuit modeling in MATLAB Simulink as Stateflow model. Modeling of a precharge based circuit using higher level model equations has been done. To determine the accuracy of the model that depends on the equations governing the behaviour of the MOSFETs, BSIM3v3 level49 equations have been considered. It also depends on the influence of the various model parameters. An efficient modeling technique has been developed for CMOS circuit with a precharge based circuit with separate pMOS/nMOS networks. The model's completeness and circuit performance requirements are formulated and reachability analysis has been performed on the model. The benefit of the present modeling technique is that Stateflow model is comparable with respect to real circuit simulation results. Though the model uses complex circuit equations, evaluation time is comparatively fast.

This thesis then presents an application of SAT based tool to find optimal values of the relevant parameters to achieve a specified circuit performance. Signal temporal logic (STL) formulas are used to specify the desired properties of continuous signals determining the parameters of the underlying model. Two optimisation algorithm have been used Nelder Mead (NM) algorithm of Breach tool and a 2D search algorithm. The circuit performance is optimised through finding a range of admissible circuit parameters. Results obtained from Breach can be visualised through Matlab Simulink. An efficient optimisation technique has been developed for CMOS circuits that determine the transistor parameters. The advantage of the optimisation technique is that a range of admissible circuit parameters are obtained.

This thesis finally presents experimentations on CMOS inverter, NAND2, NOR2 and precharge based circuit. The effectiveness of the above modeling technique has been demonstrated with a set of experimental results. The CMOS circuits have been redesigned using Spice simulator with synthesized transistor size values obtained using optimisation algorithms. Results obtained from NM and 2D search algorithms are comparable with the Spice results.

Keywords : CMOS transistor sizing, Stateflow model, precharged CMOS logic, level 49 BSIM3 MOSFET model, reachability analysis, signal temporal logic, Nelder Mead algorithm, 2D search algorithm

Contents

List of Abbreviations and Symbols

ADC	Area-Delay Curve
APE	Analog Performance Estimation
NM	Nelder Mead
CMOS	Complementary Metal-Oxide Semiconductor
DE	Differential Evolution
MOS	Metal-Oxide Semiconductor
MDE	Minimum Delay Estimation
PSO	Particle Swarm Optimization
RGA	Real-coded Genetic Algorithm
STL	Signal Temporal Logic
C_{L}	is the load capacitance
C_{dbn}	is the drain to bulk junction capacitances of nMOS transistors
C_{dbp}	is the drain to bulk junction capacitances pMOS transistors
C_{gdn}	is the gate to drain capacitances of nMOS transistors
C_{gdp}	is the gate to drain capacitances of pMOS transistors
GND	Ground
L	Channel Length of transistor
I_{p}	is the drain current through pMOS
I_{n}	is the drain current through nMOS
t_r	Rise Time
t_f	Fall Time
V_{dd}	Supply voltage
V_{ds}	voltage between drain and source
V_{dsat}	saturation voltage
V_{gs}	voltage between gate and source
V_{out}	is the output voltage
V_{th}	Threshold voltage

V_{bi}	Built-in voltage
V_{to}	Zero-bias threshold voltage
V_{FB}	flatband voltage
W	Channel width of transistor
ϕ_{f}	is bulk Fermi potential
ϕ_{ms}	is metal semiconductor work function differnce
γ	is the body effect factor
F_{l}	is the short channel factor
F_{w}	is the narrow width factor based on thick field oxide
X_{j}	is the junction depth of source and drain junction
X_{sd}	is the depletion layer width of source
X_{dd}	is the depletion layer width of drain
ϵ_{o}	is dieletric constant of vaccum
ϵ_{ox}	is dielectric constant of SiO_2
ϵ_{si}	is permitivity of Si
μ_{n}	is carrier mobility of nMOS
c_{ox}	is the gate oxide capacitance per unit area
t_{ox}	is the thickness of oxide layer
λ	is the channel-length modulation
P_{p}	is peak power at pMOS transistor
P_{n}	is peak power at nMOS transistor
P_{sc}	is short circuit power dissipation

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Chapter 1

Introduction

The most important component in today's microelectronics is the transistor. MOSFET transistors are designed as pMOS and nMOS transistors. For semiconductor devices the equivalent circuit model elements are highly nonlinear and element values are strongly dependent on DC bias, frequency, signal level and temperature. Therefore, the first step is the accurate modelling of the behaviour of the circuit on which suitable analysis can be carried out. In general there are three types of circuit models- DC models, transient models and AC models. These circuit models correspond to three basic types of circuit analysis: *i*) A DC model is a static model which evaluates the device current for a fixed voltage, not varying with time. Thus in a DC model dynamic effects such as time delay arising from the presence of energy-storage elements i.e. capacitors are ignored. *ii*) A transient model is a large-signal dynamic model that evaluates the device current when the applied voltage is varying with time. Dynamic effects arising from the charging or discharging of device storage elements, usually capacitances are included. *iii*) An AC model is a small-signal model that evaluates the current when the applied voltage variation is so small that the resulting small current variations can be expressed using linear relations. The small signal linear model is obtained from the DC model of the device. AC model is used for the frequency-domain analysis. In this work, the MOSFET models that are concerned with is the transient model and contains only capacitances as the storage elements. The performance of a device can be described in terms of mathematical equations, considering theoretical or empirical methods, or both can be used to derive a model. Physical, environmental, and operational conditions influence strongly the device characteristics. A few model parameters along with the characterization can be used to build a desired model.

Highly advanced models exist to handle deep submicron circuits [1]. However, for demonstrating the techniques developed in this work, Spice level 2

and BSIM3v3 level 49 model of MOS transistor is considered towards developing the analytical methods. There are two types of analytical models where model equations are directly derived from device physics. One type of model is based on surface potential analysis known as charge sheet models [2, 3]. These models are inherently continuous in all regions of operation of the device. The current can be accurately determined using these models, but the equations themselves are complex, thus not very suitable for circuit simulation. The second type of analytical model is the result of applying various approximations to the semiconductor equations, based upon decisions as to which physical phenomena dominate [4–6]. Thus different equations are used to represent different regions of operation of the device. The level 2 model is a second-order model of MOS device behavior and BSIM3v3 level 49 is the higher order model. Based on such second-order behavior model of MOS devices, the output waveform of a CMOS inverter driven by a step input has been reported by [7]. The accuracy of the device depends on the equations governing the behaviour of the MOSFETs at different regions and also the influence of the various model parameters. Therefore after modelling the device accurately, the second step is the parameter optimisation.

The rest of the chapter is organized as follows. Section 1.1 deals with motivation of the present work. Section 1.2 gives an overview of the present research work and highlights the specific contributions of the thesis. Finally, Section 1.3 outlines the organization of the rest of the thesis.

1.1 Motivation

Simulation is considered to be essential because conducting a complex experiment is often challenging. For instance, the computer simulation process simulates an electronic circuit, where we describe the entire circuit with a mathematical description through mathematical equations. MATLAB Simulink is one of the widely used industrial tools. It helps in modelling systems, even if they are more complex. The resulting model must be tested to detect the completeness of the model. But, such a model consists of many blocks, so the testing process becomes complex. So we have to decrease the complexity of the models to handle large models and ensure the complex models' quality. Therefore, the Stateflow designing tool of MATLAB is used to model, simulate, and analyze systems to capture the systems' event-driven behavior. Event-driven systems where the system makes a transition from one state to another state based on transition condition. Thus it confirms the completeness of the system if all accepting states in a system are reachable. The mathematical equations are a function of parameters that configures

the mathematical model to describe the dependence of the output signal. The parameter values have to be determined from a known data set using a technique called parameter optimisation.

Circuit optimisation, by way of transistor resizing and selection of other design parameters, to achieve multiple objectives is an important design goal [8]. Optimisation of design metrics such as rise time, fall time and power are important objectives for modelling CMOS circuits. The parameter optimisation requires measurements of several device parameters along with different combinations of length and width of the device (nMOS and pMOS). There is a functional relationship between device parameters and design objectives. For instance, power dissipation is related to transistor size (width, length) and load capacitor. Rise time and fall time are dependent on output capacitor and on-resistance, which need to be minimized for faster switching [9]. On-resistance of transistor can be minimized by increasing the W/L ratio of the transistor.

1.2 Overview and Contributions of the Thesis

In this work, modelling of CMOS circuits has been done in the Matlab environment by using Simulink/Stateflow designing tool and parameter optimisation using the Breach toolbox. Matlab Simulink is a modelling tool that includes Stateflow [10]. Stateflow has been studied for formal modelling [11] [12] and verification [13]. Signal temporal logic (STL) [14] formulas are used to specify the desired properties of continuous signals determining the parameters of the underlying model. Breach [15] is an analytic toolbox of Matlab which can be used to monitor and analyze the transient behavior of model based systems. Breach estimates dense sets that are reachable by the model based on simulation [16]. Breach works on STL properties [17] for a given Stateflow model and returns *false* (0), if no satisfying trace can be found; otherwise, *true* (1) is returned.

1.2.1 Contribution

An attempt has been made to utilise problem-specific features to achieve an efficient transistor sizing technique to achieve design objectives. This work has three contributions as listed below.

- Simulink Stateflow (hybrid system) modelling of transistor operation of CMOS inverter, CMOS NAND2 and CMOS NOR2 at Spice level 2 and checking the completeness of the model through reachability

analysis. The designed model is comparable with respect to the real circuit simulation results and execution time is fast.

- Simulink Stateflow (hybrid system) modelling of transistor operation of precharge based logic circuits at BSIM3v3 level 49 and checking the completness of the model. The model designed using Stateflow simulink is comparable with respect to the real circuit simulation results and execution time is fast.

- Formulation of desired circuit performance required using STL properties to capture desired properties (rise time, fall time and power). Parameter determination (transistor sizing) to achieve performance goals using the Breach tool; Nelder mead (NM) algorithm and the presented two dimensional (2D) search algorithm has been used to compare the parameters more efficiently. Using 2D search algorithm, it is possible to obtain a range of parameters with less computation time as compared to NM algorithm. The CMOS circuits are created using spice with optimised values of transistor width achieved through NM algorithm and 2D search algorithm to verify the stateflow model.

1.3 Organization of the rest of the Thesis

This section presents an outline of the organization of the rest of the thesis.
Chapter 2: Survey of literature has been presented that led to the motivation behind the present work.
Chapter 3: Hybrid Modelling of CMOS circuits (CMOS inverter, CMOS NAND2, and CMOS NOR2) as a hybrid system at spice Level 2 has been done in the Matlab environment using Simulink/Stateflow design tool. Reachability analysis has been done to confirm that the dead state is unreachable from the initial state and confirm the completeness of the model.
Chapter 4: Hybrid modelling of the dual-rail precharge circuit as a hybrid system at BSIM3v3 Level 49 have been done in the Matlab environment using Simulink/Stateflow design tool. For checking the completeness of a model, reachability analysis has been done and to confirm that the dead state is unreachable from the initial state.
Chapter 5: Formulation of desired circuit performance requires using STL formula and parameter determination to achieve performance goals using Breach tool, which attempts to find a set of parameters using the Nelder-Mead (NM) algorithms in the given ranges. The presented two dimensional (2D) search algorithm has been used to compare the parameters more efficiently.

Chapter 6: Experimental results are provided to demonstrate the effectiveness of the methodology. To verify the results achieved through the NM algorithm and proposed 2D search algorithm, the CMOS circuits have been redesigned with synthesized values of output load capacitance and transistor size using Spice simulator.
Chapter 7 : The contributions of this thesis are summarized in this chapter.

Chapter 2

Literature Survey

In this chapter, we present a comprehensive survey of the literature related to the following topics (i) modeling of digital circuits, (ii) rise time and fall time and power dissipation and (iii) optimisation techniques.

2.1 Modelling of Digital Circuits

Before the actual fabrication of a designed circuit, the circuit performance should be predicted and evaluated. A better modeling is needed to predict and evaluate the behavior of the circuit [18]. The analytical response derived by Kayssi *et al.* [19] is based on first-order model of MOS device behavior where the second-order phenomena including carrier velocity saturation effect, the carrier mobility degradation and weak inversion are kept suppressed. The models are designed using mathematical equations to improve and predict the real time behaviour of the transistors [20]. Karlsson *et al.* [21] has presented linear region model parameters of submicron transistors and neglected the parameters at saturation region. An analytical models to describe the propagation delay and the power consumption of the CMOS inverter in closed mathematical forms using nanometer MOS transistors has been proposed by Chaourani *et al.* [22]. However, in this models the current of the short-circuiting transistor has been neglected and uses simplified transistor current expressions. Consoli *et al.* [23] has reported piecewise linear approximation and handles only nine parameters. Other analytical models which employ heavy approximations and still several physical effects i.e. channel-length modulation, drain-induced barrier lowering were neglected [24]. Sheu *et al.* [25] has reported a model where the second order mobility reduction factor is neglected. The behaviours of a circuit depend on the transistor channel length and width through complex high orders of equations. For a complex circuit, the relationships between the design parameters and the

performance parameters becomes complicated [26] [27]. The design of nano scale CMOS inverter using 45 nm Berkeley Predictive Technology model parameters [28] for simulation as well as for evaluating the cost function using PSO is reported by [29]. The transistor geometries (the channel length and channel width) are considered to be the design parameters and form the design space which is to be explored in order to obtain an optimal solution point [30]. In [31], an improved analytical propagation delay model has been presented, but it neglects the channel length modulation effect, which is important for deep submicron technologies. The MOSFET threshold voltage (V_{th}) is an essential device parameter. For an accurate design, its value must be hold within certain limits and thus it is important that V_{th} be modeled accurately [32]. A two - dimensional analytical solution was devoloped by using the charge sharing approach [33] or simplifying Poisson's equation in the depletion region [34] [35]. They used simple geometrical division of the depletion layer in the substrate to derive the expressions of threshold voltage.

Dual-Rail Logic [36] [37] is a pre-charged based circuit technique which is used to improve the speed of CMOS circuits.

In this work, stateflow modelling of complex circuits considering the short channel effects of MOS transistor using Spice level2 and BSIM3v3 level 49 will be taken into account for higher accuracy modelling of short-channel devices.

2.2 Rise Time and Fall Time and Power Dissipation

CMOS circuits can be optimized in a number of ways, such as device model selection, and transistor sizing. For a given technology, a small change in the transistor size leads to a remarkable change in the characteristics of a circuit. Therefore, an appropriate transistor sizing method is necessary for acceptable circuit performance. So, to achieve the best circuit performance one should attempt to minimize power and minimize delay where both power and delay parameters are functions of the transistor size. For a certain technology, the channel lengths of all transistors are fixed at the minimal feature size [38]. So, the only variable to be optimized is the channel width of each transistor. Several approaches have been applied in transistor sizing, one being a mathematical optimisation method [39] [40]. In this method, the transistor sizing problem is formulated as a constrained nonlinear mathematical program. Two algorithms, MDE (Minimum Delay Estimation) and ADC (Area-Delay Curve), are based on logical effort. Once the delay is optimized using MDE algorithm, the ADC algorithm optimizes area-delay product. Hence, in these

algorithms the delay performance is the target parameter and power is not optimized. The work [41] shows how these algorithms can size the transistors without running a heuristic sizing tool by calculating the minimum achievable delay and the cost of achieving a target delay. A transistor sizing tool for speed, area, and power optimisation of static CMOS circuits is reported by Dutta *et al.* [42].

The first analytical expressions for the output waveform including the effect of the input slope were presented by Hedenstiema *et al.* [43], where the influence of short circuit current was neglected. These expressions were extended by Kayssi *et al.* [19] for the exponential input waveform, step input and ramp input, but still short circuit current was not included. The differential equation that describes the discharge of the load capacitor was solved for a rising input ramp considering the currents through both transistors [44]. However, in the case where the nMOS device is saturated and the PMOS device is in the linear region, the quadratic term of the current through the pMOS device was neglected. Vemuru *et al.* [45] derived an expression for the output waveform, which includes this term of the pMOS current, using a power series to approximate the solution of the differential equation. However, only the first five terms of the series were calculated, and a recursion form for the calculation of higher order terms in order to obtain better accuracy, was not considered.

The power dissipation is a strong function of transistor sizing which affects capacitance. Thus, sources of power consumption such as short-circuit currents can be minimized by designing circuit and transistor sizing accurately. Transistor sizing also affects time constant of the gate due to the parasitic capacitors. Veendrick *et al.* report a scheme for short circuit power [46] based on the Shichman and Hodges model [47]. However, they do not consider the load capacitance. Bisdounis *et al.* [48] includes the load capacitance into account but rely on a long channel model of the transistor. In this work the scheme presented by Chatzigeorgiou *et al.* [49] has been used which takes the load capacitance into account. Low-power design is an important objective for which transistor sizing in a static CMOS layout may be utilised [50]. Low power CMOS digital design with optimal supply voltage and transistor sizing is reported by Anantha et al. [51], where they argue that smallest possible W/L ratios minimise power dissipation.

In this work, the channel length of all transistors are kept fixed. Transistor width is optimized such that minimum rise time, minimum fall time and minimum power are achieved.

2.3 Optimisation techniques

Optimisation techniques are used to explore the optimal choice of design parameters. The BSIM models derived for MOS transistors use a very large number of parameters. These parameters are extracted for particular operating conditions [52]. Optimum parameter extraction is of utmost significance in modern technology [53] [54]. Fast Diffusion [55] algorithim is a global optimisation methods solves on multidimensional continuous space. The algorithm performs a greedy search and a random search and finds the global minimum with a practical success rate. The extraction process in these method is fast and difficult because they use complex derivatives in the calculation. However, the author find it difficult to guess the initial parameter and to know if the current point is near the global minimum. One of the other known simple models, called α-power model [56], ignores the channel-length modulation effect and is also unable to predict an accurate value for the drain current in the saturation region. The n-th power [57] model is an extension of the alpha-power law MOSFET model. The n-th power model considers the channel-length modulation but the accuracy of this method may not be satisfactory as the model equation is simple. An analog performance estimation (APE) tool for integrated circuits described in [58] takes the design parameters i.e transistor sizes of an circuit as inputs and determines its performance parameters (e.g., power consumption). The accuracy of the estimated results with respect to circuit-level simulation results is not good because the model equations are based on simple MOS models (SPICE level 1 equations). There are other optimisation techniques used for different optimisation problems such as genetic algorithm (GA), differential evolution (DE) algorithm, and particle swarm optimisation (PSO) [59]. These evolutionary algorithms are based on global search. Evolutionary algorithms such as real coded genetic algorithm (RGA) and DE have been employed to achieve the optimal switching characteristics of CMOS inverter [60]. Design of CMOS inverter having symmetric output waveform with equal rise time (t_{r}) and fall time (t_{f}) is investigated using PSO [61] [62]. These algorithms do not guarantee in finding an optimal solution . In contrast, a local search algorithm is good at finding a good solution [63]. However, these algorithms reported an optimiation technique for single objective with simple model.

In this work, formulation of desired circuit performance requirements has been done using STL properties to capture desired properties (rise time, fall time and power) using Breach tool, which attempts to find a set of parameters using the Nelder-Mead (NM) algorithms in the given ranges. The presented two dimensional (2D) search algorithm has been used to compare the parameters more efficiently.

Chapter 3

Modelling and Analysis of Transistor Operation using Spice MOS Level 2 Model

Model based design is a methodology to analyze the behaviour of the systems. Many industries use MATLAB and Mathematica to design and simulate tool sets. MATLAB Simulink is a software for modelling, simulating and analyzing dynamic systems. It supports linear and non-linear systems, modeled in continuous time. Stateflow is a component of MATLAB Simulink which captures the discrete control states. Stateflow designing tool in Matlab Simulink is a platform to model deterministic models. In this work, CMOS circuits have been modeled in Matlab environment by using Simulink/Stateflow designing tool. For checking the completness of a model reachabiltiy analysis has been done to confirm that the dead state state is unreachable from the intial state.

3.1 Modelling Mechanism and Completeness

3.1.1 Stateflow

Stateflow is a graphical designing tool that works with Simulink to model and simulate event-driven systems. It provides a graphical editor on which the Stateflow graphical objects are dragged from the design palette and creates finite state machines. In this work, the stateflow model has been generated automatically using Matlab Script. The standard definition of stateflow [64] is given below.

Definition 1. The stateflow diagram can be defined as a triple $\langle$ S, T, V $\rangle$ where: *i)* $S = \{S_{\mathrm{a}}, S_{\mathrm{b}}, ...S_{\mathrm{n}}\}$ is a finite set of states in a model.

ii) T is a finite set of transitions between two states. *iii*) V is a finite set of continuous variables $V_1, V_2, ...V_n$ of the model.

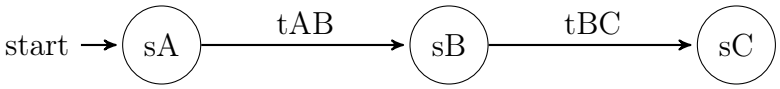


Figure 3.1: State Diagram.

- **States** During simulation a state is either active or inactive; it changes in response to events and conditions. The activity status of a state determines the state's behavior. During entry actions state becomes active, and exit actions are executed when a state becomes inactive. Let us use Figure 3.1, part of Stateflow diagram as an example. For instance, state counter contains the states sA, sB, sC. The order can be assigned manually by designer or determined automatically by the Stateflow simulator. States have labels which denote the state's name, entry actions, during actions, exit actions and on event actions [65].
  - **Entry actions** define the actions to be taken initially, i.e. when the state is entered or activated.
  - **During actions** define the set of actions to be taken when the state is already active and some event occurs.
  - **Exit actions** define the set of actions to be taken when the state becomes inactive from active.
  - **On event actions** define the actions to be taken when a state is active and the mentioned event occurs.
- **Transitions**

  A transition is a edge that links one graphical object with other objects (a state or a junction). A transition between two states represents a mode change from the source state to the destination state. The source state is the state where transition begins and the destination state is the state where the transition ends. One end of a transition is attached to a source state and the other end to a destination state. In the state diagram as shown in Figure 3.1, transition tAB has a source state sA and destination state sB. When the source state and the destination state are same, then it is a self-loop transition that causes the source state to become inactive and immediately thereafter become active. So, the occurrence of an event causes a transition to take place. Transition

tAB in Figure 3.1 is the event required to trigger the transition from state sA to state sB. Exclusive state that is enter initially, is determined by a default transition, the default transition in the state diagram is state sA. It is a transition with no source state. The standard definition of transition is given below.

Definition 2. Transition is a septuple $\langle$ src, dst, C, A_{cond}, A_{trans}, ord, int $\rangle$ where:

src is the source state (or null in case of a default transition).

dst is the destination state

C is the finite set of conditions states in a model

A_{trans} is finite list of transition actions for the states in a model

A_{cond} is finite list of conditions for transition actions for the states in a model

ord is an execution order of the transitions in a model

init is the parent state (or null).

A transition is identified by its label which consists of events, conditions, condition actions, and transition actions in the following format.

$$event[condition]\{condition\_action\}/transition\_action$$

- **Event** specifies the event that should cause the transition to occur.
- **Condition** specifies a boolean expression that needs to be evaluated to true for the transition to take place.
- **Condition action** specifies the action to be immediately executed when the condition evaluates to true.
- **Transition action** specifies the action to be executed when the transi- tion destination has been determined to be valid provided the condition is true, if specified.

There can be different types of transition in Stateflow like inner transitions, transitions between substates etc. For instance, we consider only flat Stateflows without junctions, history junctions.

- **Events** Events drive the stateflow chart execution but are nongraphical objects. All events that affect the chart must be defined to the stateflow. An event can handle a transition or an action to be executed. Events are executed in a top-down manner i.e. starting from

the event's parent in the hierarchy. Events are created and modified using the Model Explorer, and they can exist at any level in the hierarchy. Events have properties such as a scope which is display box with respect to simulation time. The scope defines whether the event is

  - Local to the Stateflow chart
  - An input to the chart from its Simulink model
  - An output from the chart to its Simulink model
  - Exported to a (code) destination external to the chart and Simulink model
  - Imported from a code source external to the chart and Simulink model

- **Data** In stateflow, data objects are used to store numerical values. They are nongraphical objects and are thus not represented directly in a Stateflow. The data objects for Stateflow can be created and modified in the Model Explorer. Data objects have a property called scope that defines whether the data object is

  - Local to the Stateflow chart
  - An input to the chart from its Simulink model
  - An output from the chart to its Simulink model
  - Nonpersistent temporary data
  - Parameter which is defined in the MATLAB workspace
  - A constant
  - Exported to a (code) destination external to the chart and Simulink model
  - Imported from a code source external to the chart and Simulink model

- **Conditions** A condition is a Boolean expression specifying a transition to occurs, given that the specified expression is true. In the stateflow diagram , the transition from A to B occurs if the transition condition is true.

- **Actions** Actions take place as part of Stateflow execution. The action can be executed either as part of a transition from one state to another or based on the activity status of a state.

- **Solvers** The Simulink models are simulated by solvers which computes the states of the system at successive time steps over a specified time span. A designer can specify the simulation type of a model as fixed-step simulation where the states of the system is calculated at fixed intervals. This size of the interval is called the step size. If the step size small, more the accuracy of simulation is more and also the time required to simulate. On the other hand, specifying variable step simulation for a system, the time step reduces where the system change is rapid and increases the time step. This approach is useful for models with rapidly changing or piecewise continuous states and maintains a specified level of accuracy. The solvers can be broadly categorised into continuous solvers and discrete solvers. Continuous solvers compute the state of a system in the present time step using numerical integration from the system's state in the previous time steps and the state derivatives. Continuous solvers depend on the model to compute the values of the discrete states at each time step. Discrete solvers primarily solve discrete models and compute the next simulation time step for a model. Discrete solvers do not compute continuous states and they depend on the model blocks to update the model discrete states. Accordingly, Simulink provides a set of solvers, that realize a particular approach to solve a model. A designer can choose a solver for a model that is best suited. In this work, as the model has continuous states; variable-step continuous solver has been used.

3.1.2 Rechability Analysis and Completeness

A reachable state is a state that is reachable from the initial state. A model is unsafe if a single traces enters a dead state. A dead state is a rejecting or an unwanted state; once the states in a model enters the dead state there is no way to reach accepting states. Considering two states sA and sB, where sB is a step-successor of sA, $sA \rightarrow_s sB$, if either $sA \rightarrow_{ti} sB$, or there exists $sC \in C \times R^n$ such that $sA \rightarrow_{ti} sC$ and $sC \rightarrow_{tr} sA$. The state sB is said to be reachable from the state sA if $s \rightarrow_s^* sA$. A model is considered safe if unsafe states cannot be reached starting from initial safe or accepting states. The sequence of states s = (sA, sB . . . . sZ) will be called the path length 'len' connecting the states sA and sZ. If there is a path connecting sA and sZ, the path is called a cycle. State sA can be connected with any other state. Thus, a model is said to be complete if all accepting states are reachable.

3.2 Transistor Operation Modelling

In SPICE2.G [66] there are three different MOS models. The Level 1 model is the simple Shichman-Hodges model. The level 1 model is a first-order model of MOS device behavior, and second-order phenomena including carrier velocity saturation effect, the carrier mobility degradation and weak inversion are kept suppressed. The Level 3 model is a semi-empirical model specified by a set of parameters which are defined by curve-fitting rather than defining the actual physical characteristics of the device. The Level 2 model is an analytical one-dimensional model which includes most of the second-order effects of small-size devices. The accuracy of the model depends on the values of the input parameters. Therefore, it is important to understand the equations governing the circuit behaviour of the MOSFETs and also the influence of the various model parameters. So in this chapter, Level 2 model equations has been considered for modelling CMOS circuits.

3.2.1 Description of MOSFET Parameters at SPICE Level 2

According to MOSFET device, various model parameters influence the pMOS and nMOS behaviour. MOSFETs are characterized by device parameters : *i*) W and L are the channel width and channel length; *ii*) AD and AS are the drain and source area, respectively; they scale the parameters JS and C_{j} of the model. *iii*) PD and PS are the perimeters of the drain and source respectively; they multiply the junction sidewall capacitance C_{jsw} specified in F/m on the model. The MOSFETs are also characterized by derived parameter (electrical parameter) and primary parameter (processing parameter). These parameters have significant effects on the MOSFET operation as in static and dynamic (transient) mode of operation. Determining the influence of the derived parameters and primary parameters that characterize the MOSFET behaviour (nMOS transistor and pMOS transistor) depends on selection of parameter values. Designing the MOSFET with appropriate parameters enables the design of CMOS circuits with the best performance. Primary parameters are described as below

- NSUB is the substrate doping and is used in the derivation of most of the derived parameters like Gamma (γ) and zero bias threshold voltage (V_{to}).
- NSS is the effective surface charge density and is used to evaluate the flatband voltage and zero bias threshold voltage.

- NFS is the effective fast surface state density.
- NEFF is the total channel charge coefficient. It is defined when the velocity saturation is specified (VMAX) in the Level=2 model.
- TPG is the type of gate indicates whether the simulated device has a metal or polysilicon gate.

$$TPG = \begin{cases} +1, & \text{for gate type opposite to the substrate} \\ -1, & \text{for gate type same as the substrate} \\ 0, & \text{for aluminium} \end{cases}$$

Derived parameter as follows:

- V_{to} is the zero bias threshold voltage of a long and wide channel device. V_{to} is evaluated from the equation (3.1) considering the NSUB and t_{ox} are specified.

$$V_{\text{to}} = V_{\text{FB}} + 2\phi_{\text{f}} + \frac{2\sqrt{q\epsilon_{\text{si}} NSUB\phi_{\text{f}}}}{c_{\text{ox}}} \tag{3.1}$$

$$V_{\text{FB}} = \phi_{\text{ms}} - \frac{q \cdot NSS}{c_{\text{ox}}} \tag{3.2}$$

  where, V_{FB} is the flatband voltage [67] [68], q is the electron charge, ϵ_{si} is the dielectric constant os silicon (Si), c_{ox} is the gate oxide capacitance per unit area, ϕ_{ms} is the metal semiconductor work function difference, ϕ_{f} is the surface potential and NSS is surface state density and NSUB is the substrate doping density.

- Gamma (γ) is the bulk threshold parameter and represents the proportionality factor relating the change in threshold voltage to backgate bias. It is derived from the equation (3.3)

$$\gamma = \frac{\sqrt{2q\epsilon_{\text{si}} NSUB}}{c_{\text{ox}}} \tag{3.3}$$

- KP is the intrinsic transconductance parameter. It is computed by the equation (3.4), given the parameter value surface mobility (μ_{o}) and gate oxide thickness (t_{ox}) .

$$k_{\text{p}} = \mu_{\text{o}} \times c_{\text{ox}} \tag{3.4}$$

- Phi (ϕ_f) is the surface potential and is computed from the equation (3.5)

$$\phi_f = 2\frac{kT}{q}\ln\frac{NSUB}{ni} \tag{3.5}$$

- Lambda (λ) is the channel-length modulation. For Level 2 model, Lambda will compute a finite and voltage dependent output conductance defined by the equation (3.6)

$$\lambda = \frac{\Delta L}{L_{\text{eff}} \times V_{\text{ds}}} \tag{3.6}$$

where, L_{eff} is the channel length, X_D is the coefficient of depletion layer width

$$\Delta L = X_D \left[\frac{V_{\text{ds}} - V_{\text{dsat}}}{4} + \sqrt{1 + \left(\frac{V_{\text{ds}} - V_{\text{dsat}}}{4}\right)^2}\right]^{\frac{1}{2}}$$

The parameters are further classified into the properties of carriers in the conductive channel.

- μ_{o} is the surface mobllity at low gate voltsges.
- UCRIT is the critical field for mobility Degradation and is the limit at which the surface mobility μ_{o} starts decreasing according to the empirical relation.
- UEXP is the critic and field exponent for the empirical formula which characterizes the degradation of the surface mobility.
- UTRA is the transverse field coefficient for the empirical mobility degradation formula.

The above four parameters are calculated in the following equation of the surface mobility degradation [69]

$$\mu_s = \mu_o \times \left[\frac{UCRIT \times \epsilon_{\text{si}}}{c_{\text{ox}}(V_{\text{gs}} - V_{\text{th}} - UTRA \times V_{\text{ds}})}\right] \tag{3.7}$$

The parameters that characterize the gate and channel of the MOSFETs are further classified as oxide characteristics, charge concentrations and mobility parameters. The gate capacitances C_{gs}, C_{gd}, C_{gb} are the overlap capac-

itances. These capacitances are constant with voltage. Capacitance model of MOSFET is explained in section 3.2.2.2

- C_{gso} is the gate source overlap capacitance per channel width.
- C_{gdo} is the gate drain overlap capacitance per channel width.
- C_{gbo} is the gate bulk overlap capacitance per channel length.

In this chapter, a model based CMOS circuits has been explained using standardised transistor operation model following level 2 [70]. These expressions were derived using current-voltage relationships originally developed for short-channel transistors, considering parasitic capacitance of the transistors. In CMOS circuits, two kinds of transistors are distinguished namely nMOS transistor and pMOS transistor as shown in Figure 3.2. Both the transistors can be in one of three operations regions: cut-off state , triode (linear) state and saturation state. In cut-off state the transistor is an open circuit. In triode state also known as ohmic state, the current is proportional to the applied voltage. In saturation state, the current is constant and independent of the applied voltage.

(a) pMOS (b) nMOS

Figure 3.2: MOS Transistors.

3.2.2 MOSFET Level 2 Model Eequations

In this work, Stateflow modelling of CMOS circuits has been carried out using standardized transistor operation for modelling at level 2 [70]. These expressions were derived using complex current-voltage relationships incorporates many of the second order effects taking into account their parasitic capacitors of the transistors. Figure 3.3 shows the CMOS inverter circuit.

3.2.2.1 DC Model

The threshold voltage equation for the SPICE Level 2 model is expressed as :

$$V_{\text{th}} = V_{\text{bi}} + \gamma F_{\text{l}} \cdot \sqrt{(2\phi_{\text{f}} + V_{\text{sb}})} \tag{3.8}$$

Device	**Cut-off**	**Triode**	**Saturation**
nMOS	$V_{\text{gsn}} < V_{\text{tn}}$	1. $V_{\text{gsn}} > V_{\text{tn}}$	1. $V_{\text{gsn}} > V_{\text{tn}}$
	$V_{\text{in}} < V_{\text{tn}}$	$V_{\text{in}} > V_{\text{tn}}$	$V_{\text{in}} > V_{\text{tn}}$
		2.$V_{\text{dsn}} < V_{\text{gsn}} - V_{\text{tn}}$	2. $V_{\text{dsn}} > V_{\text{gsn}} - V_{\text{tn}}$
		$V_{\text{out}} - V_{\text{ss}} < V_{\text{in}} - V_{\text{ss}} - V_{\text{tn}}$	$V_{\text{out}} - V_{\text{ss}} > V_{\text{in}} - V_{\text{ss}} - V_{\text{tn}}$
		$V_{\text{out}} < V_{\text{in}} - V_{\text{tn}}$	$V_{\text{out}} > V_{\text{in}} - V_{\text{tn}}$
pMOS	$V_{\text{gsp}} > V_{\text{tp}}$	1.$V_{\text{gsp}} < V_{\text{tp}}$	1.$V_{\text{gsp}} < V_{\text{tp}}$
	$V_{\text{in}} - V_{\text{dd}} > V_{\text{tp}}$	$V_{\text{in}} < V_{\text{dd}} + V_{\text{tp}}$	$V_{\text{in}} < V_{\text{dd}} + V_{\text{tp}}$
	$V_{\text{in}} > V_{\text{dd}} + V_{\text{tp}}$	2.$V_{\text{dsp}} > V_{\text{gsp}} - V_{\text{tp}}$	2.$V_{\text{dsp}} < V_{\text{gsp}} - V_{\text{tp}}$
		$V_{\text{out}} - V_{\text{dd}} > V_{\text{in}} - V_{\text{dd}} - V_{\text{tp}}$	$V_{\text{out}} - V_{\text{dd}} < V_{\text{in}} - V_{\text{dd}} - V_{\text{tp}}$
		$V_{\text{out}} > V_{\text{in}} - V_{\text{tp}}$	$V_{\text{out}} < V_{\text{in}} - V_{\text{tp}}$

Table 3.1: Three Modes of Operation of Transistor

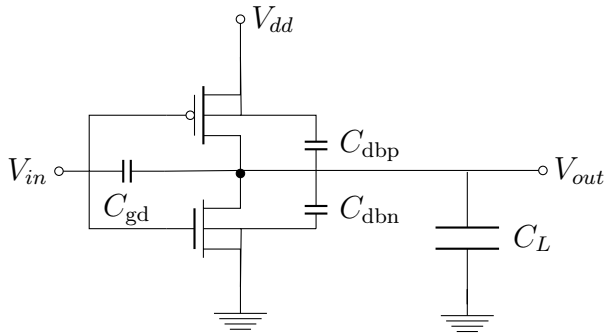


Figure 3.3: CMOS inverter circuit.

The built in voltage for narrow channel is expressed as:

$$V_{\mathrm{bi}} = V_{\mathrm{to}} - \gamma\sqrt{2\phi_{\mathrm{f}}} + F_{\mathrm{w}} \cdot (2\phi_{\mathrm{f}} + V_{\mathrm{sb}}) \tag{3.9}$$

where, V_{to} is the zero-bias threshold voltage of a long channel device, ϕ_{f} is bulk Fermi potential, γ is the body effect factor, F_{l} is the short channel factor given by equation (3.10), F_{w} is the narrow width factor based on thick field oxide model given by equation (4.7).

$$\begin{aligned} F_{\mathrm{l}} =& 1 - \left[\frac{X_{\mathrm{j}}}{2\mathrm{L}} \cdot \left(\sqrt{1 + \frac{2X_{\mathrm{sd}}}{X_{\mathrm{j}}}} - 1\right) + \right. \\ & \left. \frac{X_{\mathrm{j}}}{2\mathrm{L}} \cdot \left(\sqrt{1 + \frac{2X_{\mathrm{dd}}}{X_{\mathrm{j}}}} - 1\right)\right] \end{aligned} \tag{3.10}$$

where, X_{j} is the junction depth of source and drain junction, X_{sd} is the depletion layer width of source given by equation (3.12), X_{dd} is the depletion layer width of drain given by equation (3.13).

$$F_{\mathrm{w}} = \left(\frac{\pi}{4}\right) \cdot \left(\frac{\epsilon_{\mathrm{o}} \cdot \epsilon_{\mathrm{si}}}{C_{\mathrm{ox}}}\right) \cdot \frac{G_{\mathrm{w}}}{\mathrm{W}} \tag{3.11}$$

where, G_{w} is the channel width factor

$$X_{\mathrm{sd}} = \sqrt{\frac{2 \cdot \epsilon_{\mathrm{o}} \cdot \epsilon_{\mathrm{si}}}{q \cdot N_{\mathrm{b}}} \cdot (\phi_{\mathrm{bi}} + V_{\mathrm{sb}})} \tag{3.12}$$

$$X_{\mathrm{dd}} = \sqrt{\frac{2 \cdot \epsilon_{\mathrm{o}} \cdot \epsilon_{\mathrm{si}}}{q \cdot N_{\mathrm{b}}} \cdot (\phi_{\mathrm{bi}} + V_{\mathrm{ds}} + V_{\mathrm{sb}})} \tag{3.13}$$

where, ϵ_{o} is dieletric constant of vaccum, N_{b} is substrate doping.

The saturation voltage of nMOS transistor V_{dsatn} is expressed as :

$$\begin{aligned} V_{\mathrm{dsatn}} =& \frac{V_{\mathrm{gsx}} - V_{\mathrm{bi}}}{\eta} + \frac{1}{2}\left(\frac{\gamma F_{\mathrm{l}}}{\eta}\right)^2 \left[1 - \left[1 + 4\left(\frac{\eta}{\gamma F_{\mathrm{l}}}\right)^2 \right.\right. \\ & \left.\left. \times \left(\frac{V_{\mathrm{gsx}} - V_{\mathrm{bi}}}{\eta} + 2\phi_{\mathrm{f}} + V_{\mathrm{sb}}\right)\right]^{\frac{1}{2}}\right] \end{aligned} \tag{3.14}$$

where,

$$V_{\text{gsx}} = \begin{cases} V_{\text{gsn}}, & \text{if } V_{\text{gsn}} \geq V_{\text{tn}} \\ V_{\text{tn}}, & \text{if } V_{\text{gsn}} < V_{\text{tn}} \end{cases}$$

The drain current I_{Dn}, through nMOS transistor is given by three modes of operation.

a) Cut-off mode: When no drain current flows through the transistor i.e. $I_{\text{Dn}} = 0$ occurs when $V_{\text{gsn}} < V_{\text{tn}}$.
Where, V_{gsn} is gate to source voltage , V_{tn} is threshold voltage.

b) Triode Mode: It is a linear region also known as ohmic region. It occurs when $V_{\text{gsn}} > V_{\text{tn}}$ and $V_{\text{dsn}} < V_{\text{dsatn}}$. The current equation (3.15) in triode mode is given as:

$$\begin{aligned} I_{\text{Dn}} =& (\beta) \cdot [(V_{\text{gsn}} - V_{\text{bi}} - \frac{1}{2}\eta V_{\text{dsn}}) \cdot V_{\text{dsn}} - \\ & \frac{2}{3}\gamma F_{\text{l}} \cdot \{(V_{\text{dsn}} + 2\phi_{\text{f}} + V_{\text{sb}})^{\frac{3}{2}} - (2\phi_{\text{f}} + V_{\text{sb}})^{\frac{3}{2}}\}] \end{aligned} \tag{3.15}$$

where,

$$\beta = k_{\text{p}} \cdot \frac{W_{\text{n}}}{L_{\text{effn}}}$$

$$c_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}$$

c_{ox} is the gate oxide capacitor per unit area, ϵ_{ox} is dielectric constant of SiO_2, t_{ox} is the thickness of oxide layer, W_{n} channel width, L_{effn} is effective channel length.

c) Saturation Mode: For a constant V_{gsn}, with the increase of drain to source voltage the channel gets pinched off at the drain, $V_{\text{dsn}} > V_{\text{dsatn}}$. The current equation (3.16) in saturation mode is given as:

$$\begin{aligned} I_{\text{Dn}} =& (\beta) \cdot [(V_{\text{gsn}} - V_{\text{bi}} - \frac{1}{2}\eta V_{\text{dsatn}}) \cdot V_{\text{dsatn}} - \\ & \frac{2}{3}\gamma F_{\text{l}} \cdot \{(V_{\text{dsatn}} + 2\phi_{\text{f}} + V_{\text{sb}})^{\frac{3}{2}} - (2\phi_{\text{f}} + V_{\text{sb}})^{\frac{3}{2}}\}] \end{aligned} \tag{3.16}$$

Similarly, the drain current I_{Dp}, through pMOS transistor is given by three modes of operation.

a) Cut-off mode: When no drain current flows through the transistor i.e. $I_{\mathrm{Dp}} = 0$ occurs when $V_{\mathrm{gsp}} > V_{\mathrm{tp}}$.
Where, V_{gsp} is gate to source voltage of pMOS, V_{tp} is threshold voltage of pMOS.

b) Triode Mode: It is a linear region. It occurs when $V_{\mathrm{gsp}} < V_{\mathrm{tp}}$ and $V_{\mathrm{dsp}} > V_{\mathrm{dsatp}}$. The current equation (3.17) in triode mode is given as:

$$\begin{aligned} I_{\mathrm{Dp}} =& (\beta) \cdot [(V_{\mathrm{gsp}} - V_{\mathrm{bi}} - \frac{1}{2}\eta V_{\mathrm{dsp}}) \cdot V_{\mathrm{dsp}} - \\ & \frac{2}{3}\gamma F_{\mathrm{l}} \cdot \{(V_{\mathrm{dsp}} + 2\phi_{\mathrm{f}} + V_{\mathrm{sb}})^{\frac{3}{2}} - (2\phi_{\mathrm{f}} + V_{\mathrm{sb}})^{\frac{3}{2}}\}] \end{aligned} \tag{3.17}$$

where,

$$\beta = k_{\mathrm{p}} \cdot \frac{W_{\mathrm{p}}}{L_{\mathrm{effp}}}$$

$$c_{\mathrm{ox}} = \frac{\epsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}}$$

c_{ox} is the gate oxide capacitor per unit area, ϵ_{ox} is dielectric constant of SiO_2, t_{ox} is the thickness of oxide layer, W_{p} channel width of pMOS, L_{effp} is effective channel length of pMOS.

c) Saturation Mode: For a constant V_{gsp}, with the increase of drain to source voltage the channel gets pinched off at the drain, $V_{\mathrm{dsp}} < V_{\mathrm{dsatp}}$. The current equation (3.18) in saturation mode is given as:

$$\begin{aligned} I_{\mathrm{Dp}} =& (\beta) \cdot [(V_{\mathrm{gsp}} - V_{\mathrm{bi}} - \frac{1}{2}\eta V_{\mathrm{dsatp}}) \cdot V_{\mathrm{dsatp}} - \\ & \frac{2}{3}\gamma F_{\mathrm{l}} \cdot \{(V_{\mathrm{dsatp}} + 2\phi_{\mathrm{f}} + V_{\mathrm{sb}})^{\frac{3}{2}} - (2\phi_{\mathrm{f}} + V_{\mathrm{sb}})^{\frac{3}{2}}\}] \end{aligned} \tag{3.18}$$

For nMOS, $V_{\mathrm{gs}} = V_{\mathrm{in}}$, $V_{\mathrm{ds}} = V_{\mathrm{out}}$ and for pMOS, $V_{\mathrm{gs}} = V_{\mathrm{in}} - V_{\mathrm{dd}}$, $V_{\mathrm{ds}} = V_{\mathrm{out}} - V_{\mathrm{dd}}$. Equation (3.19) is the differential equation that describes the circuit operation of the CMOS inverter.

$$\begin{aligned} & I_{\mathrm{n}} + C_{\mathrm{dbn}} \cdot \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} = I_{\mathrm{p}} - C_{\mathrm{L}} \cdot \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} + \\ & (C_{\mathrm{gdn}} + C_{\mathrm{gdp}}) \cdot \left(\frac{\mathrm{d}V_{\mathrm{in}}}{\mathrm{d}t} - \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t}\right) - C_{\mathrm{dbp}} \cdot \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} \end{aligned} \tag{3.19}$$

where, C_{L} is the load capacitor, C_{dbn}, C_{dbp} are the drain to bulk junction capacitances of nMOS and pMOS transistors, C_{gdn}, C_{gdp} are the gate to drain

capacitances of nMOS and pMOS transistors, V_{out} is the output voltage, I_{p} is the drain current through pMOS and I_{n} is the drain current through nMOS.

3.2.2.2 Capacitance Model

The capacitances associated with a MOSFET include *i*) overlap capacitances (C_{gso}, C_{gdo}, C_{gbo}) *ii*) junction capacitances (C_{j}, C_{jsw}) *iii*) intrinsic capacitances (C_{gs}, C_{gd}, C_{gb}).

$C_{\text{gs}} = C_{\text{gsc}} + C_{\text{gso}}$ $C_{\text{gd}} = C_{\text{gdc}} + C_{\text{gdo}}$ $C_{\text{gb}} = C_{\text{gbc}}$ $C_{\text{sb}} = C_{\text{sdiff}}$; $C_{\text{db}} = C_{\text{ddiff}}$

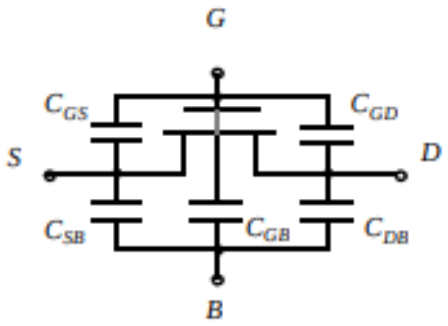


Figure 3.4: MOSFET capacitance model.

When the transistor is in the cutoff region in which the gate to source voltage is less than the threshold voltage i.e. $V_{gs} < V_{th}$, no channel exists and the gate-to-channel capacitance C_{gc} appears between gate and the bulk. In the triode region with $V_{gs} > V_{th}$ and a small voltage, V_{ds}, is applied between drain and source, an inversion layer is formed which acts as a conductor between source and drain. Consequently $C_{gb} = 0$ as the body electrode is shielded from the gate by the channel. In this region the capacitance is distributed between source and drain evenly. In saturation mode, the channel is pinched off. The gate-drain capacitance and the gate-body capacitance is approximately zero. All the capacitance hence is between gate and source. Gate capacitive effects in three operating regions of MOSFET including overlapping capacitances are tabulated in the Table 3.2.

The drain to bulk capacitance is expressed as

$$C_{\text{db}} = K_{\text{eq}} \cdot A_{\text{D}} \cdot C_{\text{j}} + K_{\text{eqsw}} \cdot P_{\text{D}} \cdot C_{\text{jsw}} \tag{3.20}$$

where, C_{j} is the bottom junction capacitance , C_{jsw} side-wall junction capacitance.

Capacitance	Cut-off	Triode	Saturation
Cgb	CoxWL	0	0
Cgd	CoxWL_D	1/2CoxWL+CoxWL_D	CoxWL_D
Cgs	CoxWL_D	1/2CoxWL+CoxWL_D	2/3CoxWL+CoxWL_D

Table 3.2: MOSFET Gate capacitance

3.3 Stateflow Modelling of CMOS Inverter

Based on the combination of the pMOS and nMOS transistors, the total number of possible locations is $3 \times 3 = 9$, the Stateflow model of the CMOS inverter has nine locations: *sA*, *sB*, *sC*, *sD*, *sE*, *sF*, *sG*, *sH* and *sI*. Among these, locations *sH* and *sI*, where both the transistors are in cut-off or in triode states, should not be reachable. If V_{tn} is greater than V_{in}, nMOS transistor is in the cut-off, to make pMOS transistor to stay in the cut-off, V_{tp} has to be greater than V_{in}, which is not possible because pMOS stays in cut-off for V_{in} greater than $V_{\text{dd}} - V_{\text{tp}}$. Similarly, if V_{out} is greater than V_{dsatp}, pMOS transistor is in triode, and to make nMOS transistor to stay in triode, V_{out} is greater than V_{dsatn}, which is not possible because nMOS stays in triode for V_{out} less than V_{dsatn}. The Stateflow model is considered to be safe if the dead state (*sdead*) is unreachable from the initial states [71].

The operating regions of pMOS and nMOS transistors have been summarized in Table 3.3. The Stateflow model of CMOS inverter is shown in Figure 3.7. Here, as the input voltage is less than the threshold voltage, the initial location is *sA* where the CMOS inverter remains for T_1 time. The operation

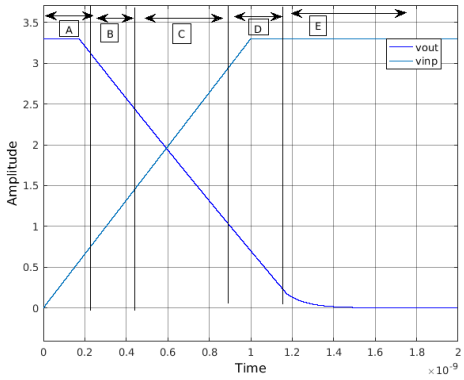


Figure 3.5: Rising ramp input (CMOS inverter).

of the inverter is explained by applying rising and falling ramp inputs, shown in Figure 3.5 and Figure 3.6, respectively. As a result transitions happend

Region	**pMOS state**	**nMOS state**
A	Triode	Cut-off
B	Triode	Saturation
C	Saturation	Saturation
D	Saturation	Triode
E	Cut-off	Triode
F	Saturation	Cut-off
G	Cut-off	Saturation
H	Cut-off	Cut-off
I	Triode	Triode
Dead	-	-

Table 3.3: Operating regions of pMOS and nMOS transistors of CMOS inverter

through the following regions.
Region A: ⟨pMOS: Triode, nMOS: Cut-off⟩
Invariant: $A_{\text{inv}} = (V_{\text{in}} < V_{\text{tn}}) \wedge (V_{\text{in}} \leq V_{\text{dd}} - V_{\text{tp}})$
V_{tn} is threshold voltage of nMOS. Only the pMOS is conducting to charge the load capacitor towards V_{dd}. When V_{in} increases so that $V_{\text{in}} = V_{\text{tn}}$ a transition occurs to region B. Operation here is governed by equation (3.21) where, ⟨pMOS: Triode, nMOS: Cut-off⟩.

$$I_{\text{p}} - C_{\text{dbp}} \cdot \frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}t} + (C_{\text{gdp}}) \cdot \left(\frac{\mathrm{d}V_{\text{in}}}{\mathrm{d}t} - \frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}t} \right) = C_{\text{L}} \cdot \frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}t} \tag{3.21}$$

Region B: ⟨pMOS: Triode, nMOS: Saturation ⟩
Invariant: $(V_{\text{in}} \geq V_{\text{tn}}) \wedge (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatp}}) \wedge (V_{\text{out}} \geq V_{\text{dsatn}})$.
If the invariant is violated, transition is made to region A or to region C. Operation here is governed by equation (3.19) where, ⟨pMOS: Triode, nMOS: Saturation⟩.
Region C: ⟨pMOS: Saturation, nMOS: Saturation ⟩
Invariant: $(V_{\text{in}} \geq V_{\text{tn}}) \wedge (V_{\text{out}} \geq V_{\text{dsatn}}) \wedge (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}})$.
If the invariant is violated, transition is made to region B or to region D. Operation here is governed by equation (3.19) where, ⟨pMOS: Saturation, nMOS:Saturation⟩.
Region D: ⟨pMOS: Saturation, nMOS: Triode ⟩.
Invariant: $(V_{\text{in}} \geq V_{\text{tn}}) \wedge (V_{\text{out}} \leq V_{\text{dsatn}}) \wedge (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}})$.

If the invariant is violated, transition is made to region C or to region E. Operation here is governed by equation (3.19) where, ⟨pMOS: Saturation, nMOS:Triode⟩.
Region E: ⟨pMOS: Cut-off, nMOS: Triode⟩.
Invariant: $E_{\text{inv}} = (V_{\text{in}} \geq V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{in}} \geq V_{\text{tn}})$
V_{tp} is threshold voltage of pMOS. Only the nMOS is conducting, causing the load capacitor to discharge through it. If the invariant is violated, transition is made to region D. Operation here is governed by equation (3.22) where, ⟨pMOS: Cut-off, nMOS:Triode⟩.

$$I_{\text{n}} + C_{\text{dbn}} \cdot \frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}t} = (C_{\text{gdn}}) \cdot \left(\frac{\mathrm{d}V_{\text{in}}}{\mathrm{d}t} - \frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}t} \right) - C_{\text{L}} \cdot \frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}t} \tag{3.22}$$

Region Dead: This region is reached if a transition from a legal region of the system to another legal region, as described above, is not possible.
Invariant:

Transition A to Dead (tADead): $\neg(V_{\text{in}} > V_{\text{tn}} \vee (V_{\text{in}} > V_{\text{dd}} - V_{\text{tp}})) \wedge \neg(V_{\text{in}} \leq V_{\text{tn}} \vee (V_{\text{in}} \leq V_{\text{dd}} - V_{\text{tp}}))$

Transition A1 to Dead (tA1Dead): $\neg([(V_{\text{out}} \geq V_{0.1}) \vee (V_{\text{out}} \leq V_{0.1} + 0.001 \times V_{\text{dd}})]) \wedge \neg([(V_{\text{out}} \geq V_{0.9}) \vee (V_{\text{out}} \leq V_{0.9} + 0.001 \times V_{\text{dd}})])$

Transition A2 to Dead (tA2Dead): $\neg([(V_{\text{out}} \geq V_{0.9}) \vee (V_{\text{out}} \leq V_{0.9} + 0.001 \times V_{\text{dd}})]) \wedge \neg(V_{\text{in}} > V_{\text{tn}})$

Transition B to Dead (tBDead): $\neg((V_{\text{in}} < V_{\text{tn}}) \vee (V_{\text{dsatp}} > V_{\text{out}} - V_{\text{dd}})) \wedge \neg((V_{\text{dsatp}} \leq V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{in}} \geq V_{\text{tn}}))$

Transition C to Dead (tCDead): $\neg(((V_{\text{dsatp}} < V_{\text{out}} - V_{\text{dd}})) \vee (V_{\text{out}} < V_{\text{dsatn}})) \wedge \neg(((V_{\text{dsatp}} \leq V_{\text{out}} - V_{\text{dd}})) \vee (V_{\text{out}} \geq V_{\text{dsatn}}))$

Transition D to Dead (tDDead): $\neg((V_{\text{in}} > (V_{\text{dd}} - V_{\text{tp}})) \vee (V_{\text{out}} > V_{\text{dsatn}})) \wedge \neg((V_{\text{out}} \leq V_{\text{dsatn}}) \vee (V_{\text{in}} \leq (V_{\text{dd}} - V_{\text{tp}})))$

Transition E to Dead (tEDead): $\neg((V_{\text{in}} > (V_{\text{dd}} - V_{\text{tp}})) \vee (V_{\text{in}} \leq (V_{\text{dd}} - V_{\text{tp}}))) \wedge \neg([(V_{\text{out}} \geq V_{0.9}) \vee (V_{\text{out}} \leq V_{0.9} + 0.001 \times V_{\text{dd}})])$

Transition E1 to Dead (tE1Dead): $\neg([(V_{\text{out}} \geq V_{0.1}) \vee (V_{\text{out}} \leq V_{0.1} + 0.001 \times V_{\text{dd}})]) \wedge \neg([(V_{\text{out}} \geq V_{0.9}) \vee (V_{\text{out}} \leq V_{0.9} + 0.001 \times V_{\text{dd}})])$

Transition E2 to Dead (tE2Dead): $\neg([(V_{\text{out}} \geq V_{0.1}) \vee (V_{\text{out}} \leq V_{0.1} + 0.001 \times V_{\text{dd}})]) \wedge \neg((V_{\text{in}} > (V_{\text{dd}} - V_{\text{tp}})) \vee (V_{\text{in}} \leq (V_{\text{dd}} - V_{\text{tp}})))$.

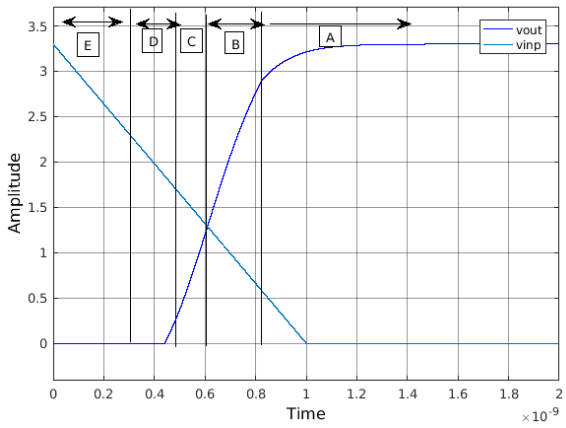


Figure 3.6: Falling ramp input (CMOS inverter).

The operation of the inverter is analysed by applying falling ramp input shown in Figure 3.6. The initial location is *sE* as the input is greater than the threshold voltage. The CMOS inverter spends T_1 time interval at location *sE*. Followed by a transition to location *sD*, location *sC*, location *sB* and finally to location *sA*. From location *sA* a transition to location *sA1* takes place as explained below.
Region A1: ⟨pMOS: Triode, nMOS: Cut-off⟩
Invariant: $((V_{\text{out}} \geq 0.1 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.1 \times V_{\text{dd}} + 0.001 \times V_{\text{dd}})) \wedge A_{\text{inv}}$
Only the pMOS is conducting to charge the load capacitor.
Region A2: ⟨pMOS: Triode, nMOS: Cut-off⟩
Invariant: $((V_{\text{out}} \geq 0.9 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.9 \times V_{\text{dd}} + 0.001 \times V_{\text{dd}})) \wedge A_{\text{inv}}$
Regions A1 and A2 form narrow bands to capture the rise time, i.e. when output voltage rises from 10% of supply voltage to 90% of supply voltage.
Region E1: ⟨pMOS: Cut-off, nMOS: Triode ⟩
Invariant: $((V_{\text{out}} \geq 0.9 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.9 \times V_{\text{dd}} + 0.001 \times V_{\text{dd}})) \wedge E_{\text{inv}}$
Region E2: ⟨pMOS: Cut-off, nMOS: Triode⟩.
Invariant: $((V_{\text{out}} \geq 0.1 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.1 \times V_{\text{dd}} + 0.001 \times V_{\text{dd}})) \wedge E_{\text{inv}}$
Regions E1 and E2 form narrow bands to capture the fall time, i.e. when output voltage falls from 90% of supply voltage to 10% of supply voltage.

3.4 Stateflow Model of CMOS NAND2

In CMOS design, the two-input NAND gate consists of two nMOS in series connected to two pMOS in parallel. The static two-input NAND gate is shown in Figure 3.8. Series transistors and parallel transistors of the same

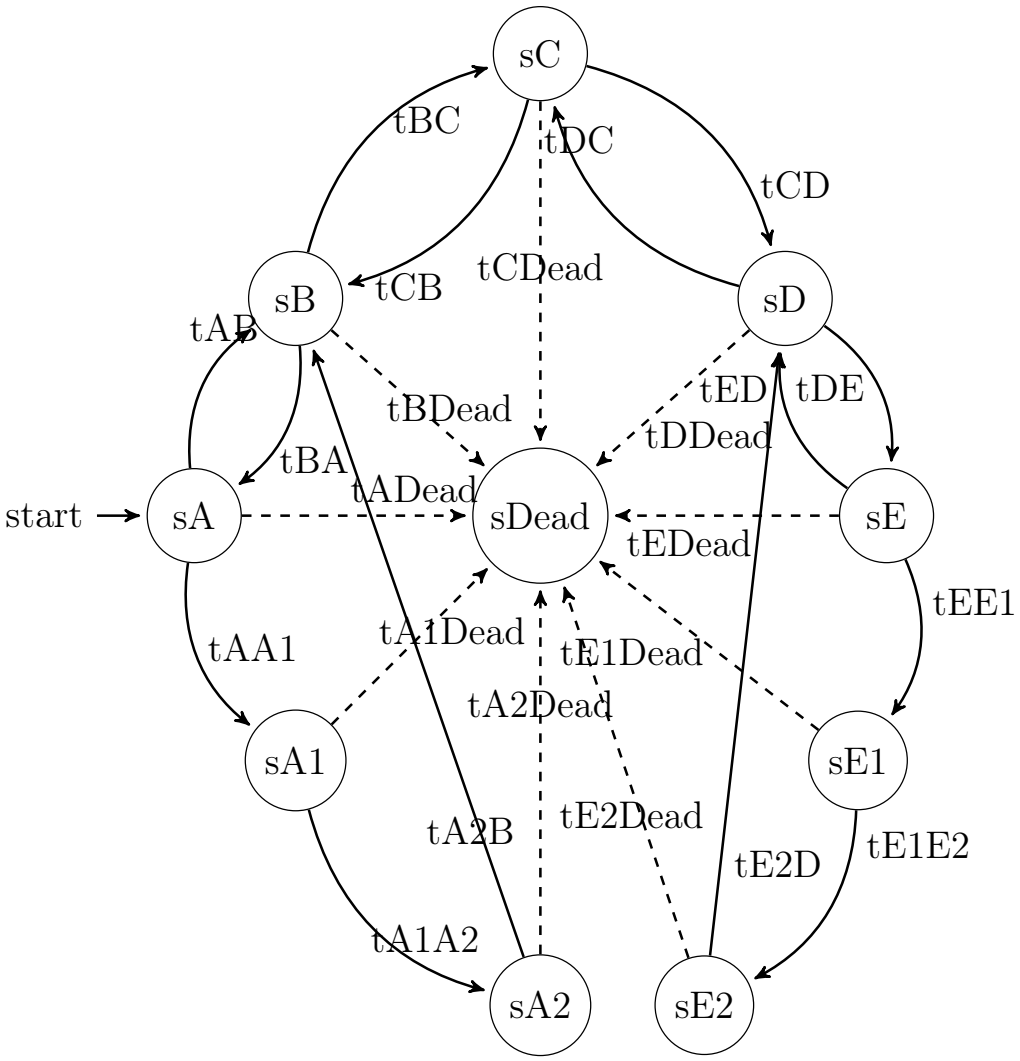


Figure 3.7: Stateflow model of CMOS inverter.

type have equal sizes to have the same conductivity. Both the transistors P_1 and P_2 in the pull-up network conducts simultaneously for $V_{\text{inA}} = V_{\text{inB}} = 0$, representing a strong pull-up and provide a connection between V_{dd} and V_{out} to pull V_{out} to logic '1'. Similarly, both the transistors N_1 and N_2 in the pull-down network conducts simultaneously for $V_{\text{inA}} = V_{\text{inB}} = 1$, representing a strong pull-down and provide a connection between ground (GND) and V_{out} to pull V_{out} to logic '0'. The truth table for CMOS NAND2 is tabulated in Table 3.4. Based on the combination of the pMOS and

V_{inA}	V_{inB}	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

Table 3.4: Truth table of CMOS NAND2

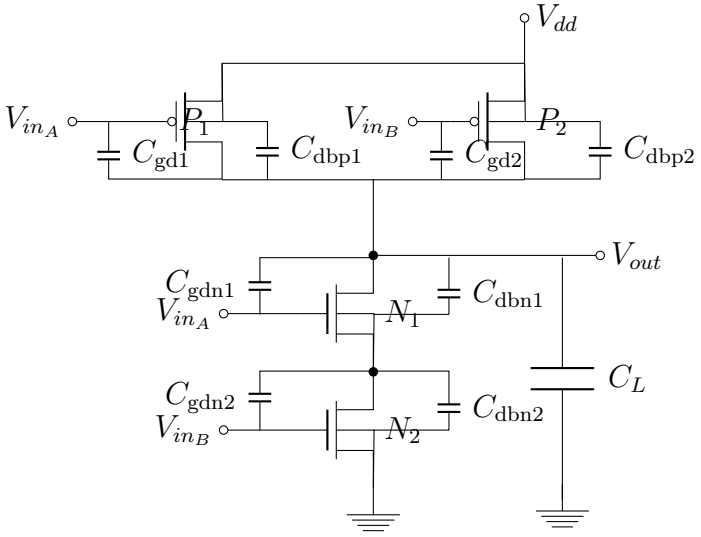


Figure 3.8: CMOS NAND2 circuit.

nMOS transistors, the Stateflow model of the CMOS NAND2 has nineteen locations *sA*, *sA1*, *sA2*, *sB*, *sC*, *sD*, *sD1*, *sD2*, *sE*, *sH*, *sI*, *sJ*, *sK*, *sN*, *sO*, *sP*, *sQ*, *sT*, *sU*. For checking that the unsafe state is unreachable, a dead (*sDead*) location has been modeled in the model. It has been confirmed that all the

accepting states are reachable. The Stateflow model of CMOS NAND2 is shown in Figure 3.9. Four possible input combinations has been considered that switch the output of the gate from high-to-low :

Case 1 : $V_{\text{inA}} = V_{\text{inB}} = 0 \rightarrow 1$,

Case 2 : $V_{\text{inA}} = 1$, $V_{\text{inB}} = 0 \rightarrow 1$,

Case 3 : $V_{\text{inB}} = 1$, $V_{\text{inA}} = 0 \rightarrow 1$,

Case 4 : $V_{\text{inA}} = 0 \rightarrow 1$, $V_{\text{inB}} = 1 \rightarrow 0$.

The output waveform is shown in Chapter 6 under Section 6.2. Depending upon the input, the model have three different initial locations as *sA*, *sB* and *sC*. The input combination that has been excluded which does not switch the output of the gate from high-to-low, i.e. if one of the input is low (logic '0'), independent with the other input, the output is always high (logic '1'). The input combination that has been excluded : *i*) Case 5 : V_{inA}=0, V_{inB}=0→1 and *ii*) Case 6 : V_{inA}=0→1, V_{inB}=0

To derive the stateflow model, the differential equation has been solved by applying the Kirchhoff's current law at the output node. As the nMOS transistors are in series and considering both the nMOS transistors to be active, the current through nMOS N_1 is given by (3.23) and current through nMOS N_2 is given by (3.24).

$$\begin{aligned} I_{\text{Dn1}} =& (\beta) \cdot [(V_{\text{gsn}} - V_1 - V_{\text{bi}} - \frac{1}{2}\eta(V_{\text{dsn}} - V_1)) \cdot (V_{\text{dsn}} - V_1) - \\ & \frac{2}{3}\gamma F_{\text{l}} \cdot \{((V_{\text{dsn}} - V_1) + 2\phi_{\text{f}} + V_{\text{sb}})^{\frac{3}{2}} - (2\phi_{\text{f}} + V_{\text{sb}})^{\frac{3}{2}}\}] \end{aligned} \tag{3.23}$$

$$\begin{aligned} I_{\text{Dn2}} =& (\beta) \cdot [(V_{\text{gsn}} - V_{\text{bi}} - \frac{1}{2}\eta V_1) \cdot V_1 - \\ & \frac{2}{3}\gamma F_{\text{l}} \cdot \{(V_1 + 2\phi_{\text{f}} + V_{\text{sb}})^{\frac{3}{2}} - (2\phi_{\text{f}} + V_{\text{sb}})^{\frac{3}{2}}\}] \end{aligned} \tag{3.24}$$

As the pMOS transistors are in parallel and considering both the pMOS transistors to be active, the voltage is same across each pMOS transistor. The current through pMOS P_1 is given by (3.25) and current through pMOS P_2 is given by (3.26).

Region	**pMOS state**		**nMOS state**	
	P_1	P_2	N_1	N_2
A	Triode	Triode	Cut-off	Cut-off
B	Triode	Cut-off	Cut-off	Triode
C	Cut-off	Triode	Triode	Cut-off
D	Cut-off	Cut-off	Triode	Triode
E	Triode	Triode	Saturation	Saturation
F	Triode	Triode	Cut-off	Saturation
G	Triode	Triode	Saturation	Cut-off
H	Triode	Cut-off	Saturation	Triode
I	Triode	Saturation	Saturation	Triode
J	Cut-off	Triode	Triode	Saturation
K	Saturation	Saturation	Saturation	Saturation
L	Triode	Saturation	Cut-off	Saturation
M	Saturation	Triode	Saturation	Cut-off
N	Saturation	Cut-off	Saturation	Triode
O	Saturation	Triode	Triode	Saturation
P	Cut-off	Saturation	Triode	Saturation
Q	Saturation	Saturation	Triode	Triode
R	Triode	Saturation	Cut-off	Triode
S	Saturation	Triode	Triode	Cut-off
T	Saturation	Cut-off	Triode	Triode
U	Cut-off	Saturation	Triode	Triode
Dead	-	-	-	-

Table 3.5: Operating regions of pMOS and nMOS transistor of CMOS NAND2

$$\begin{aligned} I_{\mathrm{Dp1}} =& (\beta) \cdot [(V_{\mathrm{sgp}} - V_{\mathrm{bi}} - \frac{1}{2}\eta V_{\mathrm{sdp}}) \cdot V_{\mathrm{sdp}} - \\ & \frac{2}{3}\gamma F_{\mathrm{l}} \cdot \{(V_{\mathrm{sdp}} + 2\phi_{\mathrm{f}} + V_{\mathrm{sb}})^{\frac{3}{2}} - (2\phi_{\mathrm{f}} + V_{\mathrm{sb}})^{\frac{3}{2}}\}] \end{aligned} \tag{3.25}$$

$$\begin{aligned} I_{\mathrm{Dp2}} =& (\beta) \cdot [(V_{\mathrm{sgp}} - V_{\mathrm{bi}} - \frac{1}{2}\eta V_{\mathrm{sdp}}) \cdot V_{\mathrm{sdp}} - \\ & \frac{2}{3}\gamma F_{\mathrm{l}} \cdot \{(V_{\mathrm{sdp}} + 2\phi_{\mathrm{f}} + V_{\mathrm{sb}})^{\frac{3}{2}} - (2\phi_{\mathrm{f}} + V_{\mathrm{sb}})^{\frac{3}{2}}\}] \end{aligned} \tag{3.26}$$

Equation 3.27 is the differential equation that describes the circuit operation of the CMOS NAND2.

$$\begin{aligned} & I_{\mathrm{n1}} + C_{\mathrm{dbn1}} \cdot \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} + I_{\mathrm{n2}} + C_{\mathrm{dbn2}} \cdot \frac{\mathrm{d}V_{\mathrm{1}}}{\mathrm{d}t} = I_{\mathrm{p1}} + I_{\mathrm{p1}} - C_{\mathrm{L}} \cdot \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} + \\ & (C_{\mathrm{gdn}} + C_{\mathrm{gdp}}) \cdot (\frac{\mathrm{d}V_{\mathrm{in}}}{\mathrm{d}t} - \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t}) - (C_{\mathrm{dbp1}} + C_{\mathrm{dbp2}}) \cdot \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} \end{aligned} \tag{3.27}$$

3.4.1 Case 1 : $V_{\mathrm{inA}} = V_{\mathrm{inB}} = 0 \rightarrow 1$

The operation of the CMOS NAND2 is found to progress through the following regions for input V_{inA} and V_{inB} switching from 0→1. For case 1, the intial location is sA.

Region A: Here ⟨ pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Cut-off, nMOS N_2:Cut-off ⟩

Invariant : $A_{\mathrm{inv}} = (V_{\mathrm{inA}} < V_{\mathrm{tn}}) \wedge (V_{\mathrm{inB}} < V_{\mathrm{tn}}) \wedge (V_{\mathrm{inA}} < V_{\mathrm{dd}} - V_{\mathrm{tp}}) \wedge (V_{\mathrm{inB}} < V_{\mathrm{dd}} - V_{\mathrm{tp}})$

Only the pMOS P1 and P2 is conducting to charge the load capacitor towards V_{dd}. Therefore the only way to leave this region is by increasing V_{inA} and V_{inB} above V_{tn}, transition to region E takes place.

Region E: Here ⟨ pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Satuartion, nMOS N_2: Satuartion ⟩

Invariant :$(V_{\mathrm{inA}} > V_{\mathrm{tn}}) \wedge (V_{\mathrm{inB}} > V_{\mathrm{tn}}) \wedge (V_{\mathrm{out}} - V_{\mathrm{dd}} \geq V_{\mathrm{dsatpa}}) \wedge (V_{\mathrm{out}} - V_{\mathrm{dd}} \geq V_{\mathrm{dsatpb}}) \wedge (V_{\mathrm{out}} \geq V_{\mathrm{dsatna}}) \wedge (V_{\mathrm{out}} \geq V_{\mathrm{dsatnb}})$

If the invariant conditon is not satisfied, this region is left and transition to region K or region A takes place. Operation here is governed by equation (3.27), where ⟨ pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Satuartion, nMOS N_2: Satuartion ⟩

Region K : Here ⟨ pMOS P_1: Satuartion, pMOS P_2: Satuartion, nMOS N_1: Satuartion, nMOS N_2: Satuartion ⟩

Invariant: $(V_{\text{inA}} > V_{\text{tn}}) \wedge (V_{\text{inB}} > V_{\text{tn}}) \wedge (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{out}} \geq V_{\text{dsatna}}) \wedge (V_{\text{out}} \geq V_{\text{dsatnb}})$ (V_{dd} is supply voltage).
If the condition violates, the region is left and transition to region Q or region E takes place.
Region Q: Here ⟨ pMOS P_1: Satuartion, pMOS P_2: Satuartion, nMOS N_1: Triode, nMOS N_2: Triode ⟩
Invariant : $(V_{\text{inA}} > V_{\text{tn}}) \wedge (V_{\text{inB}} > V_{\text{tn}}) \wedge (V_{\text{out}} < V_{\text{dsatna}}) \wedge (V_{\text{out}} < V_{\text{dsatnb}}) \wedge (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}})$
Here region Q, both the pMOS transistors operates in saturation state and both the nMOS transistors operates in triode state. Violating the invariant condition, transition to region D or region K takes place.
Region D: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode ⟩
Inavriant: $D_{\text{inv}} = (V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}})$ and $(V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inA}} > V_{\text{tn}}) \wedge (V_{\text{inB}} > V_{\text{tn}})$
Only the nMOS is conducting, causing the load capacitor to discharge through it. If the invariant is violated, transition is made to region Q.
Region A1: ⟨pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Cut-off, nMOS N_2:Cut-off ⟩
Invariant: $((V_{\text{out}} \geq 0.1 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.1 \times V_{\text{dd}} + 0.001 \times V_{\text{dd}})) \wedge A_{\text{inv}}$
Only the pMOS is conducting to charge the load capacitor.
Region A2: ⟨pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Cut-off, nMOS N_2:Cut-off ⟩
Invariant: $((V_{\text{out}} \geq 0.9 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.9 \times V_{\text{dd}} + 0.001 \times V_{\text{dd}})) \wedge A_{\text{inv}}$
Regions A1 and A2 form narrow bands to capture the rise time, i.e. when output voltage rises from 10% of supply voltage to 90% of supply voltage.
Region D1: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode ⟩
Invariant: $(V_{\text{out}} \geq 0.9 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.9 \times V_{\text{dd}} + 0.001 \times V_{\text{dd}}) \wedge A_{\text{inv}} =$.
If the invariant conditon is not satisfied, this region is left and transition to region *D2* takes place.
Region D2: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode ⟩
Invariant: $(V_{\text{out}} \geq 0.1 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.1 \times V_{\text{dd}} + 0.01 \times V_{\text{dd}}) \wedge A_{\text{inv}} =$
Regions D1 and D2 form narrow bands to capture the fall time, i.e. when output voltage falls from 90% of supply voltage to 10% of supply voltage.
Region Dead: This region is reached if a transition from a legal region of the system to another legal region, as described above, is not possible.
Invariant:

Transition A to Dead (tADead): $\neg(V_{\text{inA}} > V_{\text{tn}} \vee V_{\text{inB}} > V_{\text{tn}} \vee (V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}})) \wedge \neg(V_{\text{inB}} \leq V_{\text{tn}} \vee V_{\text{inA}} \leq V_{\text{tn}} \vee (V_{\text{inA}} \leq V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} \leq V_{\text{dd}} - V_{\text{tp}}))$

Transition A1 to Dead (tA1Dead): $\neg([(V_{\text{out}} \geq V_{0.1}) \vee (V_{\text{out}} \leq V_{0.1} + 0.001 \times V_{\text{dd}})]) \wedge \neg([(V_{\text{out}} \geq V_{0.9}) \vee (V_{\text{out}} \leq V_{0.9} + 0.001 \times V_{\text{dd}})])$

Transition A2 to Dead (tA2Dead): $\neg([(V_{\text{out}} \geq V_{0.9}) \vee (V_{\text{out}} \leq V_{0.9} + 0.001 \times V_{\text{dd}})]) \wedge \neg(V_{\text{inA}} > V_{\text{tn}} \vee V_{\text{inB}} > V_{\text{tn}})$

Transition E to Dead (tEDead): $\neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{inB}} < V_{\text{tn}}) \vee (V_{\text{out}} < V_{\text{dsatna}}) \vee V_{\text{out}} < V_{\text{dsatnb}})) \wedge \neg((V_{\text{dsatpa}} \leq V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{dsatpb}} \leq V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{inA}} \geq V_{\text{tn}}) \vee (V_{\text{inB}} \geq V_{\text{tn}}) \vee (V_{\text{out}} \geq V_{\text{dsatna}}) \vee V_{\text{out}} \geq V_{\text{dsatnb}}))$

Transition K to Dead (tKDead): $\neg((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{inB}} > V_{\text{tn}}) \vee (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} \geq V_{\text{dsatna}}) \vee (V_{\text{out}} \geq V_{\text{dsatnb}})) \wedge \neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{inB}} < V_{\text{tn}}) \vee (V_{\text{dsatpa}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{dsatpb}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} \leq V_{\text{dsatna}}) \vee (V_{\text{out}} \leq V_{\text{dsatnb}}))$

Transition Q to Dead (tQDead): $\neg((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{inB}} > V_{\text{tn}}) \vee (V_{\text{out}} < V_{\text{dsatna}}) \vee (V_{\text{out}} < V_{\text{dsatnb}}) \vee (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}})) \wedge \neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{inB}} < V_{\text{tn}}) \vee (V_{\text{out}} > V_{\text{dsatna}}) \vee (V_{\text{out}} > V_{\text{dsatnb}}) \vee (V_{\text{dsatpa}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{dsatpb}} < V_{\text{out}} - V_{\text{dd}}))$

Transition D to Dead (tDDead): $\neg((V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{inB}} > V_{\text{tn}})) \wedge \neg((V_{\text{inA}} \leq V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} \leq V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} \leq V_{\text{tn}}) \vee (V_{\text{inB}} \leq V_{\text{tn}})) \wedge \neg([(V_{\text{out}} \geq V_{0.9}) \vee (V_{\text{out}} \leq V_{0.9} + 0.001 \times V_{\text{dd}})])$

Transition D1 to Dead (tD1Dead): $\neg([(V_{\text{out}} \geq V_{0.1}) \vee (V_{\text{out}} \leq V_{0.1} + 0.001 \times V_{\text{dd}})]) \wedge \neg([(V_{\text{out}} \geq V_{0.9}) \vee (V_{\text{out}} \leq V_{0.9} + 0.001 \times V_{\text{dd}})])$

Transition D2 to Dead (tD2Dead): $\neg([(V_{\text{out}} \geq V_{0.1}) \vee (V_{\text{out}} \leq V_{0.1} + 0.001 \times V_{\text{dd}})]) \wedge \neg((V_{\text{in}} > (V_{\text{dd}} - V_{\text{tp}})) \vee (V_{\text{in}} \leq (V_{\text{dd}} - V_{\text{tp}})))$

The output of CMOS NAND2 for the input $V_{\text{inA}} = 0 \rightarrow 1$ and the input $V_{\text{inB}} = 0 \rightarrow 1$ is shown in Figure 6.2a has been shown in section chapter 6.

3.4.2 Case 2 : $V_{\text{inA}} = 1$, $V_{\text{inB}} = 0 \rightarrow 1$

As input V_{inA} is high, so, pMOS P_1 is always in cut-off state and nMOS N_1 is always in triode state. The operation of the CMOS NAND2 is found to progress through the following regions for input V_{inB} switching from $0 \rightarrow 1$.

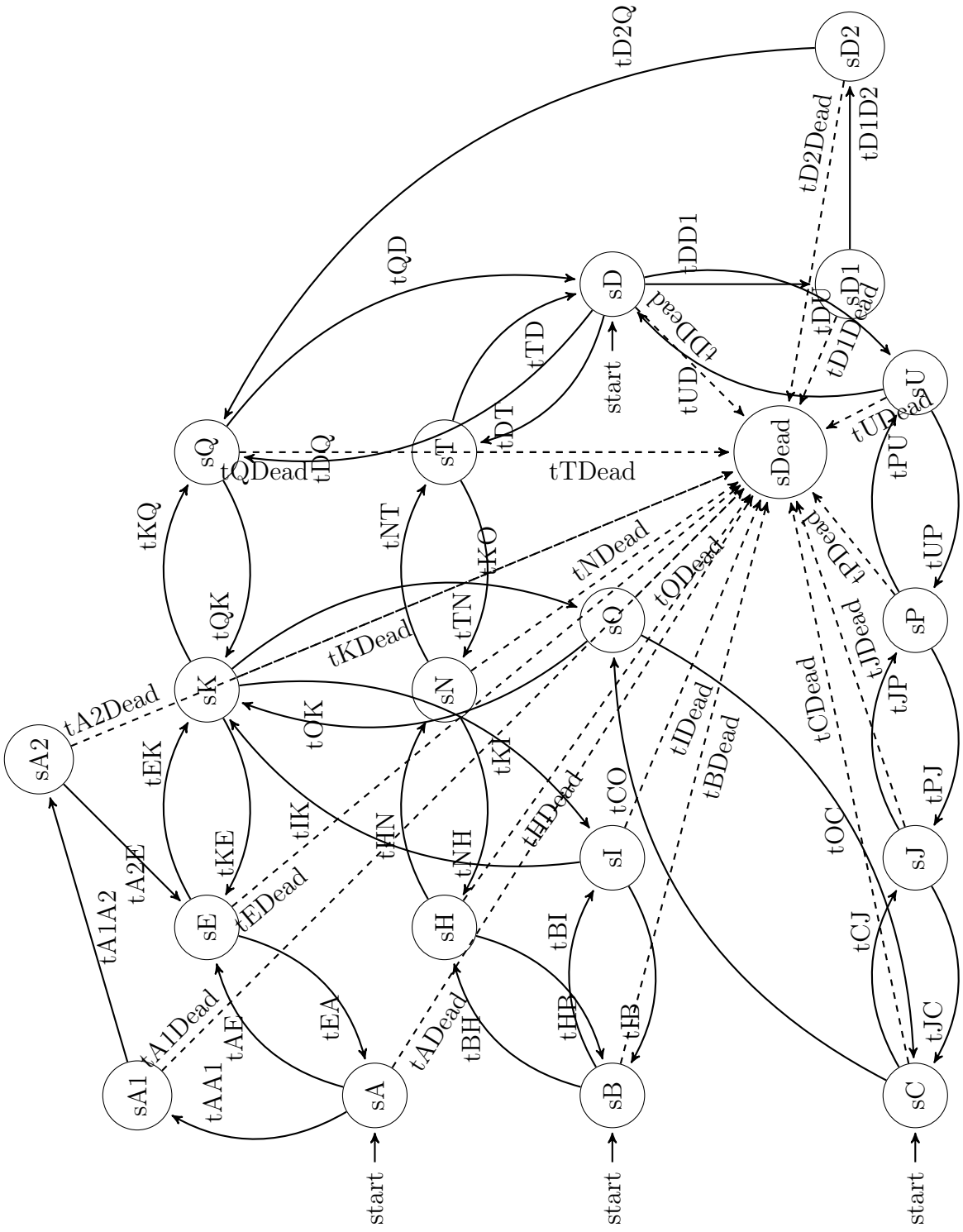


Figure 3.9: Stateflow model of CMOS NAND2.

For case 2, the initial location is *sC*.
Region C: Here ⟨ pMOS P_1: Cut-off, pMOS P_2:Triode, nMOS N_1:Triode , nMOS N_2: Cut-off ⟩
Invariant : $(V_{\text{inB}} < V_{\text{tn}}) \wedge (V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inA}} = V_{\text{dd}})$
As pmOS transistors are parallel and only one pMOS is conducting, the load capacitor is charged to V_{dd} through pMOS P_2. Therefore the only way to leave this region is by increasing V_{inB} above V_{tn}. Violating the invariant condition, transition to region J takes place.
Region J: Here ⟨ pMOS P_1: Cut-off, pMOS P_2:Triode, nMOS N_1:Triode , nMOS N_2: Saturation ⟩
Invariant : $(V_{\text{inB}} > V_{\text{tn}}) \wedge (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatpb}}) \wedge (V_{\text{out}} \geq V_{\text{dsatnb}}) \wedge (V_{\text{inA}} = V_{\text{dd}})$
If the invariant condition is not satisfied, this region is left and transition to region P or region C takes place.
Region P: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Saturation , nMOS N_1:Triode , nMOS N_2: Saturation ⟩
Invariant : $(V_{\text{inB}} > V_{\text{tn}}) \wedge V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}} \wedge (V_{\text{out}} \geq V_{\text{dsatnb}}) \wedge (V_{\text{inA}} = V_{\text{dd}})$
If the condition violates, the region is left and transition to region U orgion J takes place.
Region U: Here ⟨ pMOS P_1: Cut-off, pMOS P_2:Saturation, nMOS N_1:Triode, nMOS N_2: Triode ⟩
Invariant : $(V_{\text{inB}} > V_{\text{tn}}) \wedge (V_{\text{out}} < V_{\text{dsatnb}}) \wedge (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{inA}} = V_{\text{dd}})$
Violating the invariant condition, transition to region D or region P takes place.
Region D: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode ⟩
Inavriant: $D_{\text{inv}} = (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inB}} > V_{\text{tn}}) \wedge (V_{\text{inA}} = V_{\text{dd}})$
Region D1: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode ⟩
Invariant: $(V_{\text{out}} \geq 0.9 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.9 \times V_{\text{dd}} + 0.001 \times V_{\text{dd}}) \wedge D_{\text{inv}}$.
If the invariant conditon is not satisfied, this region is left and transition to region *D2* takes place.
Region D2: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode ⟩
Invariant: $(V_{\text{out}} \geq 0.1 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.1 \times V_{\text{dd}} + 0.01 \times V_{\text{dd}}) \wedge D_{\text{inv}}$
Region Dead: This region is reached if a transition from a legal region of the system to another legal region, as described above, is not possible.
Invariant:

Transition C to Dead (tCDead): $\neg((V_{\text{inB}} < V_{\text{tn}}) \vee (V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} = V_{\text{dd}})) \wedge \neg((V_{\text{inB}} > V_{\text{tn}}) \vee (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} = V_{\text{dd}}))$

Transition J to Dead (tJDead): $\neg((V_{\text{inB}} > V_{\text{tn}}) \vee (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatpb}}) \vee$

$(V_{\text{out}} \geq V_{\text{dsatnb}}) \vee (V_{\text{inA}} = V_{\text{dd}})) \wedge \neg((V_{\text{inB}} < V_{\text{tn}}) \vee (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatpb}}) \vee (V_{\text{out}} \leq V_{\text{dsatnb}}) \vee (V_{\text{inA}} = V_{\text{dd}}))$

Transition P to Dead (tPDead): $\neg((V_{\text{inB}} > V_{\text{tn}}) \vee V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}} \vee (V_{\text{out}} \geq V_{\text{dsatnb}}) \vee (V_{\text{inA}} = V_{\text{dd}})) \wedge \neg((V_{\text{inB}} < V_{\text{tn}}) \vee V_{\text{dsatpb}} < V_{\text{out}} - V_{\text{dd}} \vee (V_{\text{out}} \leq V_{\text{dsatnb}}) \vee (V_{\text{inA}} = V_{\text{dd}}))$

Transition U to Dead (tUDead): $\neg((V_{\text{inB}} > V_{\text{tn}}) \vee (V_{\text{out}} < V_{\text{dsatnb}}) \vee (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{inA}} = V_{\text{dd}})) \wedge \neg((V_{\text{inB}} < V_{\text{tn}}) \vee (V_{\text{out}} > V_{\text{dsatnb}}) \vee (V_{\text{dsatpb}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{inA}} = V_{\text{dd}}))$

Transition D to Dead (tDDead): $\neg((V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} > V_{\text{tn}}) \vee (V_{\text{inA}} = V_{\text{dd}})) \wedge \neg((V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} < V_{\text{tn}}) \vee (V_{\text{inA}} = V_{\text{dd}}))$

The output of CMOS NAND2 for the input $V_{\text{inA}} = 1$ and the input $V_{\text{inB}} = 0 \rightarrow 1$ is shown in Figure 6.2c has been shown in section chapter 6.

3.4.3 Case 3 : $V_{\text{inB}} = 1$, $V_{\text{inA}} = 0 \rightarrow 1$

As input V_{inB} is high, so, pMOS P_2 is always in cut-off state and nMOS N_2 is always in triode state. The operation of the CMOS NAND2 is found to progress through the following regions for input V_{inA} switching from $0 \rightarrow 1$. For case 3, the initial location is *sB*.

Region B: Here $\langle$ pMOS P_1: Triode, pMOS P_2: Cut-off, nMOS N_1: Cut-off, nMOS N_2: Triode $\rangle$

Invariant : $(V_{\text{inA}} < V_{\text{tn}}) \wedge (V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inB}} = V_{\text{dd}})$

As pmOS transistors are parallel and only one pMOS is conducting, the load capacitor is charged to V_{dd} through pMOS P_1. Therefore the only way to leave this region is by increasing V_{inA} above V_{tn}. Violating the invariant condition, transition to region H takes place.

Region H: Here $\langle$ pMOS P_1: Triode, pMOS P_2: Cut-off, nMOS N_1: Saturation, nMOS N_2: Triode $\rangle$

Invariant : $(V_{\text{inA}} > V_{\text{tn}}) \wedge (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatpa}}) \wedge (V_{\text{out}} \geq V_{\text{dsatna}}) \wedge (V_{\text{inB}} = V_{\text{dd}})$

If the invariant condition is not satisfied, this region is left and transition to region N or region B takes place.

Region N: Here $\langle$ pMOS P_1: Saturation, pMOS P_2: Cut-off, nMOS N_1: Satuartion, nMOS N_2: Triode $\rangle$

Invariant : $(V_{\text{inA}} > V_{\text{tn}}) \wedge V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}} \wedge (V_{\text{out}} \geq V_{\text{dsatna}}) \wedge (V_{\text{inB}} = V_{\text{dd}})$

If the condition violates, the region is left and transition to region T or region H takes place.

Region T: Here $\langle$ pMOS P_1: Saturation, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode $\rangle$

Invariant : $(V_{\text{inA}} > V_{\text{tn}}) \wedge (V_{\text{out}} < V_{\text{dsatna}}) \wedge (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{inB}} = V_{\text{dd}})$
Violating the invariant condition, transition to region D or region N takes place.
Region D: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode ⟩ Inavriant: $D_{\text{inv}} = (V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inA}} > V_{\text{tn}}) \wedge (V_{\text{inB}} = V_{\text{dd}})$
Region D1: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode ⟩
Invariant: $(V_{\text{out}} \geq 0.9 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.9 \times V_{\text{dd}} + 0.001 \times V_{\text{dd}}) \wedge (D_{\text{inv}})$.
If the invariant conditon is not satisfied, this region is left and transition to region *D2* takes place.
Region D2: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode ⟩
Invariant: $(V_{\text{out}} \geq 0.1 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.1 \times V_{\text{dd}} + 0.01 \times V_{\text{dd}}) \wedge (D_{\text{inv}})$
Region Dead: This region is reached if a transition from a legal region of the system to another legal region, as described above, is not possible.
Invariant:

Transition B to Dead (tBDead): $\neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} = V_{\text{dd}})) \wedge \neg((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} = V_{\text{dd}}))$

Transition H to Dead (tHDead): $\neg((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatpa}}) \vee (V_{\text{out}} \geq V_{\text{dsatna}}) \vee (V_{\text{inB}} = V_{\text{dd}})) \wedge \neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatpa}}) \vee (V_{\text{out}} \leq V_{\text{dsatna}}) \vee (V_{\text{inB}} = V_{\text{dd}}))$

Transition N to Dead (tNDead): $\neg((V_{\text{inA}} > V_{\text{tn}}) \vee V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}} \vee (V_{\text{out}} \geq V_{\text{dsatna}}) \vee (V_{\text{inB}} = V_{\text{dd}})) \wedge \neg((V_{\text{inA}} < V_{\text{tn}}) \vee V_{\text{dsatpa}} < V_{\text{out}} - V_{\text{dd}} \vee (V_{\text{out}} \leq V_{\text{dsatna}}) \vee (V_{\text{inB}} = V_{\text{dd}}))$

Transition T to Dead (tTDead): $\neg((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{out}} < V_{\text{dsatna}}) \vee (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{inB}} = V_{\text{dd}})) \wedge \neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{out}} > V_{\text{dsatna}}) \vee (V_{\text{dsatpa}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{inB}} = V_{\text{dd}}))$

Transition D to Dead (tDDead): $\neg((V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{inB}} = V_{\text{dd}})) \wedge \neg((V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{inB}} = V_{\text{dd}}))$

The output of CMOS NAND2 for the input $V_{\text{inA}} = 0 \rightarrow 1$ and the input $V_{\text{inB}} = 1$ is shown in Figure 6.2b has been shown in section chapter 6.

3.4.4 Case 4 : V_{inA}=0→1, V_{inB}=1→0

The operation of the CMOS NAND2 for case 4 ($V_{\text{inA}} = 0 \rightarrow 1$, $V_{\text{inB}} = 1 \rightarrow 0$) is found to progress through the following regions and the initial location is

sB.

Region B: Here ⟨pMOS P_1: Triode, pMOS P_2: Cut-off, nMOS N_1: Cut-off, nMOS N_2: Triode⟩

Invariant: $(V_{\text{inA}} < V_{\text{tn}}) \wedge (V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inB}} > V_{\text{tn}})$. The only way to leave this region is by increasing V_{inA} above V_{tn}. As pMOS transistors are in parallel and only one pMOS is conducting, the load capacitor is charged to V_{dd} through pMOS P_1. Therefore, violating the invariant condition, transition to region I takes place.

Region I: ⟨pMOS P_1: Triode, pMOS P_2: Saturation, nMOS N_1: Saturation, nMOS N_2: Triode⟩.

Invariant: $(V_{\text{inA}} > V_{\text{tn}}) \wedge (V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{dsatpb}} < V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{out}} > V_{\text{dsatna}})$

If the invariant conditon is not satisfied, this region is left and transition to region K or region B takes place.

Region K: ⟨pMOS P_1: Saturation, pMOS P_2: Saturation, nMOSN_1: Saturation, nMOS N_2: Saturation⟩.

Invariant: $(V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{out}} > V_{\text{dsatna}}) \wedge (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{out}} > V_{\text{dsatnb}})$

If the condition violates, the region is left and transition to region O or region I takes place.

Region O: ⟨pMOS P_1: Saturation, pMOS P_2: Triode, nMOS N_1: Triode, nMOS N_2: Saturation⟩

Invariant: $((V_{\text{inA}} > V_{\text{tn}}) \wedge (V_{\text{out}} < V_{\text{dsatna}})) \wedge (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{out}} > V_{\text{dsatnb}})$.

Violating the invariant condition, transition is made to region C or region K.

Region C: ⟨pMOS P_1: Cut-off, pMOS P_2: Triode, nMOS N_1: Triode, nMOS N_2: Cut-off⟩.

Invariant: $(V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inB}} < V_{\text{tn}}) \wedge (V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inA}} > V_{\text{tn}})$

The pMOS P_2 is in triode state and the pMOS P_1 is in the cutoff state. As pMOS transistors are in parallel and only one pMOS is conducting, the load capacitor is charged to V_{dd} through pMOS P_2.

Region Dead: This region is reached if a transition from a legal region of the system to another legal region, as described above, is not possible.

Invariant:

Transition B to Dead (tBDead): $\neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} > V_{\text{tn}})) \wedge \neg((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} < V_{\text{tn}}))$

Transition I to Dead (tIDead): $\neg((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{dsatpb}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} > V_{\text{dsatna}})) \wedge \neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} < V_{\text{dsatna}}))$

Transition K to Dead (tKDead): $\neg((V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} > V_{\text{dsatna}}) \vee (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} > V_{\text{dsatnb}})) \wedge \neg((V_{\text{dsatpa}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} < V_{\text{dsatna}}) \vee (V_{\text{dsatpb}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} < V_{\text{dsatnb}}))$

Transition O to Dead (tODead): $\neg(((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{out}} < V_{\text{dsatna}})) \vee (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{out}} > V_{\text{dsatnb}})) \wedge \neg(((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{out}} > V_{\text{dsatna}})) \vee (V_{\text{dsatpa}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{out}} < V_{\text{dsatnb}}))$

Transition C to Dead (tCDead): $\neg((V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} < V_{\text{tn}}) \vee (V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} > V_{\text{tn}})) \wedge \neg((V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} > V_{\text{tn}}) \vee (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} < V_{\text{tn}}))$

The output of CMOS NAND2 for the input $V_{\text{inA}} = 0 \rightarrow 1$ and the input $V_{\text{inB}} = 1 \rightarrow 0$ as shown in Figure 6.2d has been shown in chapter 6.

3.5 Stateflow Model of CMOS NOR2

In CMOS design, the two-input NOR gate consists of two nMOS in parallel connected to two pMOS in series. The static two-input NOR gate shown in Figure 3.10. Series transistors and parallel transistors of the same type have equal sizes to have the same conductivity. Both the transistors P_1 and P_2 in the pull-up network conducts simultaneously for V_{inA}=V_{inB}=0, representing a strong pull-up and provide a connection between V_{dd} and V_{out} to pull V_{out} to logic '1'. Similarly, both the transistors N_1 and N_2 in the pull-down network

V_{inA}	V_{inB}	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0

Table 3.6: Truth table of CMOS NOR2

conducts simultaneously for V_{inA}=V_{inB}=1, representing a strong pull-down and provide a connection between ground (GND) and V_{out} to pull V_{out} to logic '0'. Only one of the pulldown devices is on for V_{inA}=0, V_{inB}=1 or for V_{inA}=1, V_{inB}=0 resulting a weaker pull-down. The truth table for CMOS NOR2 is tabulated in Table 3.6.Based on the combination of the pMOS and nMOS transistors, the stateflow model of the CMOS NOR2 has nineteen locations *sA*, *sA1*, *sA2*, *sB*, *sC*, *sD*, *sD1*, *sD2*, *sE*, *sF*, *sG*, *sI*, *sK*, *sL*, *sM*,

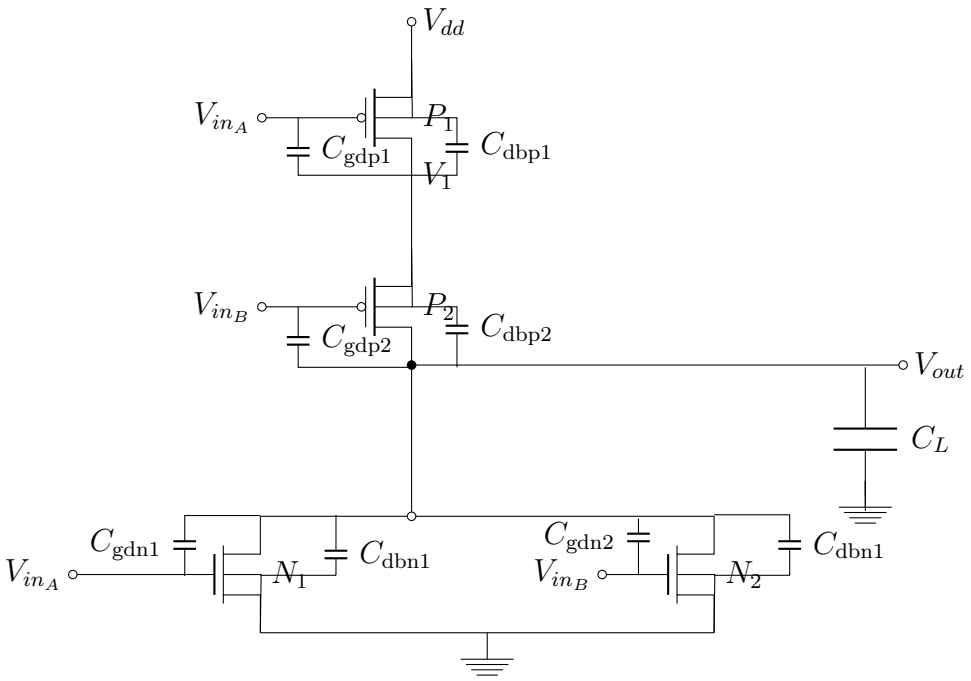


Figure 3.10: CMOS NOR2 circuit.

sO, *sQ*, *sR*, *sS*. For checking that the unsafe state is unreachable, a dead (*sDead*) location has been created in the model and has been confirmed all the accepting states are reachable. The Stateflow model of CMOS NOR2 is shown in Figure 3.11. In this model, the intial location is *sA*. The operating

Region	**pMOS state**		**nMOS state**	
	P_1	P_2	N_1	N_2
A	Triode	Triode	Cut-off	Cut-off
B	Triode	Cut-off	Cut-off	Triode
C	Cut-off	Triode	Triode	Cut-off
D	Cut-off	Cut-off	Triode	Triode
E	Triode	Triode	Saturation	Saturation
F	Triode	Triode	Cut-off	Saturation
G	Triode	Triode	Saturation	Cut-off
H	Triode	Cut-off	Saturation	Triode
I	Triode	Saturation	Saturation	Triode
J	Cut-off	Triode	Triode	Saturation
K	Saturation	Saturation	Saturation	Saturation
L	Triode	Saturation	Cut-off	Saturation
M	Saturation	Triode	Saturation	Cut-off
N	Saturation	Cut-off	Saturation	Triode
O	Saturation	Triode	Triode	Saturation
P	Cut-off	Saturation	Triode	Saturation
Q	Saturation	Saturation	Triode	Triode
R	Triode	Saturation	Cut-off	Triode
S	Saturation	Triode	Triode	Cut-off
T	Saturation	Cut-off	Triode	Triode
U	Cut-off	Saturation	Triode	Triode
Dead	-	-	-	-

Table 3.7: Operating regions of pMOS and nMOS transistor of CMOS NOR2

regions of pMOS and nMOS transistors have been summarized in Table 3.7. Series transistors and parallel transistors of the same type have equal sizes to have the same conductivity. Four possible input combinations has been considered that switch the output of the gate from high-to-low :

Case 1 A=B= 0→1

Case 2 A=0, B=0→1

Case 3 B=0, A=0→1

Case 4 A=0→1, B=1→0.

The output waveform is shown in Chapter 6 under section 6.3. The input combination that has been excluded which does not switch the output of the gate from high-to-low, i.e. if one of the input is high (logic '1'), independent with the other input, the output is always low (logic '0'). The input combination that has been excluded : *i*) Case 5 : $V_{\rm inA}$=1, $V_{\rm inB}$=0→1 and *ii*) Case 6 : $V_{\rm inA}$=0→1, $V_{\rm inB}$=1.

To derive the stateflow model, the differential equation has been solved by applying the Kirchhoff's current law at the output node. As the nMOS transistors are in parallel and considering both the nMOS transistors to be active, the current through nMOS N_1 is given by (3.28) and current through nMOS N_2 is given by (3.29).

$$\begin{aligned} I_{\rm Dn1} =&(\beta)\cdot[(V_{\rm gsn}-V_{\rm bi}-\frac{1}{2}\eta V_{\rm dsn})\cdot V_{\rm dsn}- \\ &\frac{2}{3}\gamma F_{\rm l}\cdot\{(V_{\rm dsn}+2\phi_{\rm f}+V_{\rm sb})^{\frac{3}{2}}-(2\phi_{\rm f}+V_{\rm sb})^{\frac{3}{2}}\}] \end{aligned} \tag{3.28}$$

$$\begin{aligned} I_{\rm Dn2} =&(\beta)\cdot[(V_{\rm gsn}-V_{\rm bi}-\frac{1}{2}\eta V_{\rm dsn})\cdot V_{\rm dsn}- \\ &\frac{2}{3}\gamma F_{\rm l}\cdot\{(V_{\rm dsn}+2\phi_{\rm f}+V_{\rm sb})^{\frac{3}{2}}-(2\phi_{\rm f}+V_{\rm sb})^{\frac{3}{2}}\}] \end{aligned} \tag{3.29}$$

As the pMOS transistors are in series and considering both the pMOS transistors to be active, the voltage is the same across each pMOS transistor. The current through pMOS P_1 is given by (3.30) and current through pMOS P_2 is given by (3.31).

$$\begin{aligned} I_{\rm Dp1} =&(\beta)\cdot[(V_{\rm sgp}-V_{\rm bi}-\frac{1}{2}\eta(V_{\rm dd}-V_1))\cdot(V_{\rm dd}-V_1)- \\ &\frac{2}{3}\gamma F_{\rm l}\cdot\{((V_{\rm dd}-V_1)+2\phi_{\rm f}+V_{\rm sb})^{\frac{3}{2}}-(2\phi_{\rm f}+V_{\rm sb})^{\frac{3}{2}}\}] \end{aligned} \tag{3.30}$$

$$I_{\mathrm{Dp2}} = (\beta) \cdot [(V_{\mathrm{sgp}} - V_1 - V_{\mathrm{bi}} - \frac{1}{2}\eta(V_1 - V_{\mathrm{sdp}})) \cdot (V_1 - V_{\mathrm{sdp}}) - \frac{2}{3}\gamma F_1 \cdot \{((V_1 - V_{\mathrm{sdp}}) + 2\phi_{\mathrm{f}} + V_{\mathrm{sb}})^{\frac{3}{2}} - (2\phi_{\mathrm{f}} + V_{\mathrm{sb}})^{\frac{3}{2}}\}] \tag{3.31}$$

Equation 3.32 is the differential equation that describes the circuit operation of the CMOS NOR2.

$$I_{\mathrm{Dn1}} + I_{\mathrm{Dn2}} + (C_{\mathrm{dbn1}} + C_{\mathrm{dbn2}}) \cdot \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} = I_{\mathrm{Dp1}} + I_{\mathrm{Dp1}} - C_{\mathrm{L}} \cdot \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} + (C_{\mathrm{gdn}} + C_{\mathrm{gdp}}) \cdot (\frac{\mathrm{d}V_{\mathrm{in}}}{\mathrm{d}t} - \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t}) - C_{\mathrm{dbp1}} \cdot \frac{\mathrm{d}V_1}{\mathrm{d}t} + C_{\mathrm{dbp2}} \cdot \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} \tag{3.32}$$

3.5.1 Case 1 : $V_{\mathbf{inA}} = V_{\mathbf{inB}} = \mathbf{0 \rightarrow 1}$

The operation of the CMOS NOR2 is found to progress through the following regions for input V_{inA} and V_{inB} switching from 0→1. For case 1, the intial location is sA.

Region A: Here ⟨ pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Cut-off, nMOS N_2: Cut-off ⟩

Invariant : $A_{\mathrm{inv}} = (V_{\mathrm{inA}} < V_{\mathrm{tn}}) \wedge (V_{\mathrm{inB}} < V_{\mathrm{tn}}) \wedge (V_{\mathrm{inA}} < V_{\mathrm{dd}} - V_{\mathrm{tp}}) \wedge (V_{\mathrm{inB}} < V_{\mathrm{dd}} - V_{\mathrm{tp}})$

Only the pMOS is conducting to charge the load capacitor towards V_{dd}. Therefore the only way to leave this region is by increasing V_{inA} and V_{inB} above V_{tn}. Violating the invariant condition, transition to region E takes place.

Region E: Here ⟨ pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Satuartion, nMOS N_2: Satuartion ⟩

Invariant :$(V_{\mathrm{inA}} > V_{\mathrm{tn}}) \wedge (V_{\mathrm{inB}} > V_{\mathrm{tn}}) \wedge (V_{\mathrm{out}} - V_{\mathrm{dd}} \geq V_{\mathrm{dsatpa}}) \wedge (V_{\mathrm{out}} - V_{\mathrm{dd}} \geq V_{\mathrm{dsatpb}}) \wedge (V_{\mathrm{out}} \geq V_{\mathrm{dsatna}}) \wedge (V_{\mathrm{out}} \geq V_{\mathrm{dsatnb}})$

If the invariant conditon is not satisfied, this region is left and transition to region K or region A takes place. Operation here is governed by equation (3.32) where, ⟨ pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Satuartion, nMOS N_2: Satuartion ⟩

Region K: Here ⟨ pMOS P_1: Satuartion, pMOS P_2: Satuartion, nMOS N_1: Satuartion, nMOS N_2: Satuartion ⟩

Invariant: $(V_{\mathrm{inA}} > V_{\mathrm{tn}}) \wedge (V_{\mathrm{inB}} > V_{\mathrm{tn}}) \wedge (V_{\mathrm{dsatpa}} > V_{\mathrm{out}} - V_{\mathrm{dd}}) \wedge (V_{\mathrm{dsatpb}} > V_{\mathrm{out}} - V_{\mathrm{dd}}) \wedge (V_{\mathrm{out}} \geq V_{\mathrm{dsatna}}) \wedge (V_{\mathrm{out}} \geq V_{\mathrm{dsatnb}})$

If the invariant condition violates, the transition to region Q or to region

E is made. Operation here is governed by equation (3.32) where, ⟨ pMOS P_1: Satuartion, pMOS P_2: Satuartion, nMOS N_1: Satuartion, nMOS N_2: Satuartion ⟩

Region Q: Here ⟨ pMOS P_1: Satuartion, pMOS P_2: Satuartion, nMOS N_1: Triode, nMOS N_2: Triode ⟩

Invariant : $(V_{\text{inA}} > V_{\text{tn}}) \wedge (V_{\text{inB}} > V_{\text{tn}}) \wedge (V_{\text{out}} < V_{\text{dsatna}}) \wedge (V_{\text{out}} < V_{\text{dsatnb}}) \wedge (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}})$

If the invariant is violated, transition is made to region D or region K. Operation here is governed by equation (3.32) where, ⟨ pMOS P_1: Satuartion, pMOS P_2: Satuartion, nMOS N_1: Triode, nMOS N_2: Triode ⟩

Region D: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode ⟩

Inavriant: $D_{\text{inv}} = (V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}})$ and $(V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inA}} > V_{\text{tn}}) \wedge (V_{\text{inB}} > V_{\text{tn}})$

Only the nMOS is conducting, causing the load capacitor to discharge through it. If the invariant is violated, transition is made to region Q.

Region A1: ⟨pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Cut-off, nMOS N_2:Cut-off ⟩

Invariant: $((V_{\text{out}} \geq 0.1 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.1 \times V_{\text{dd}} + 0.001 \times V_{\text{dd}})) \wedge A_{\text{inv}}$

Only the pMOS is conducting to charge the load capacitor.

Region A2: ⟨pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Cut-off, nMOS N_2:Cut-off ⟩

Invariant: $((V_{\text{out}} \geq 0.9 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.9 \times V_{\text{dd}} + 0.001 \times V_{\text{dd}})) \wedge A_{\text{inv}}$

Regions A1 and A2 form narrow bands to capture the rise time, i.e. when output voltage rises from 10% of supply voltage to 90% of supply voltage.

Region D1: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode ⟩

Invariant: $(V_{\text{out}} \geq 0.9 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.9 \times V_{\text{dd}} + 0.001 \times V_{\text{dd}}) \wedge D_{\text{inv}}$.

If the invariant conditon is not satisfied, this region is left and transition to region *D2* takes place.

Region D2: Here ⟨ pMOS P_1: Cut-off, pMOS P_2: Cut-off, nMOS N_1: Triode, nMOS N_2: Triode ⟩

Invariant: $(V_{\text{out}} \geq 0.1 \times V_{\text{dd}}) \wedge (V_{\text{out}} \leq 0.1 \times V_{\text{dd}} + 0.01 \times V_{\text{dd}}) \wedge D_{\text{inv}}$

Regions D1 and D2 form narrow bands to capture the fall time, i.e. when output voltage falls from 90% of supply voltage to 10% of supply voltage.

Region Dead: This region is reached if a transition from a legal region of the system to another legal region, as described above, is not possible.

Invariant:

Transition A to Dead (tADead): $\neg(V_{\text{inA}} > V_{\text{tn}} \vee V_{\text{inB}} > V_{\text{tn}} \vee (V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}})) \wedge \neg(V_{\text{inB}} \leq V_{\text{tn}} \vee V_{\text{inA}} \leq V_{\text{tn}} \vee (V_{\text{inA}} \leq$

$V_{dd} - V_{tp}) \vee (V_{inB} \leq V_{dd} - V_{tp}))$

Transition A1 to Dead (tA1Dead): $\neg([(V_{out} \geq V_{0.1}) \vee (V_{out} \leq V_{0.1} + 0.001 \times V_{dd})]) \wedge \neg([(V_{out} \geq V_{0.9}) \vee (V_{out} \leq V_{0.9} + 0.001 \times V_{dd})])$

Transition A2 to Dead (tA2Dead): $\neg([(V_{out} \geq V_{0.9}) \vee (V_{out} \leq V_{0.9} + 0.001 \times V_{dd})]) \wedge \neg(V_{inA} > V_{tn} \vee V_{inB} > V_{tn})$

Transition E to Dead (tEDead): $\neg((V_{inA} < V_{tn}) \vee (V_{dsatpa} > V_{out} - V_{dd}) \vee (V_{dsatpb} > V_{out} - V_{dd}) \vee (V_{inB} < V_{tn}) \vee (V_{out} < V_{dsatna}) \vee V_{out} < V_{dsatnb})) \wedge \neg((V_{dsatpa} \leq V_{out} - V_{dd}) \vee (V_{dsatpb} \leq V_{out} - V_{dd}) \vee (V_{inA} \geq V_{tn}) \vee (V_{inB} \geq V_{tn}) \vee (V_{out} \geq V_{dsatna}) \vee V_{out} \geq V_{dsatnb}))$

Transition K to Dead (tKDead): $\neg((V_{inA} > V_{tn}) \vee (V_{inB} > V_{tn}) \vee (V_{dsatpa} > V_{out} - V_{dd}) \vee (V_{dsatpb} > V_{out} - V_{dd}) \vee (V_{out} \geq V_{dsatna}) \vee (V_{out} \geq V_{dsatnb})) \wedge \neg((V_{inA} < V_{tn}) \vee (V_{inB} < V_{tn}) \vee (V_{dsatpa} < V_{out} - V_{dd}) \vee (V_{dsatpb} < V_{out} - V_{dd}) \vee (V_{out} \leq V_{dsatna}) \vee (V_{out} \leq V_{dsatnb}))$

Transition Q to Dead (tQDead): $\neg((V_{inA} > V_{tn}) \vee (V_{inB} > V_{tn}) \vee (V_{out} < V_{dsatna}) \vee (V_{out} < V_{dsatnb}) \vee (V_{dsatpa} > V_{out} - V_{dd}) \vee (V_{dsatpb} > V_{out} - V_{dd})) \wedge \neg((V_{inA} < V_{tn}) \vee (V_{inB} < V_{tn}) \vee (V_{out} > V_{dsatna}) \vee (V_{out} > V_{dsatnb}) \vee (V_{dsatpa} < V_{out} - V_{dd}) \vee (V_{dsatpb} < V_{out} - V_{dd}))$

Transition D to Dead (tDDead): $\neg((V_{inA} > V_{dd} - V_{tp}) \vee (V_{inB} > V_{dd} - V_{tp}) \vee (V_{inA} > V_{tn}) \vee (V_{inB} > V_{tn})) \wedge \neg((V_{inA} \leq V_{dd} - V_{tp}) \vee (V_{inB} \leq V_{dd} - V_{tp}) \vee (V_{inA} \leq V_{tn}) \vee (V_{inB} \leq V_{tn})) \wedge \neg([(V_{out} \geq V_{0.9}) \vee (V_{out} \leq V_{0.9} + 0.001 \times V_{dd})])$

Transition D1 to Dead (tD1Dead): $\neg([(V_{out} \geq V_{0.1}) \vee (V_{out} \leq V_{0.1} + 0.001 \times V_{dd})]) \wedge \neg([(V_{out} \geq V_{0.9}) \vee (V_{out} \leq V_{0.9} + 0.001 \times V_{dd})])$

Transition D2 to Dead (tD2Dead): $\neg([(V_{out} \geq V_{0.1}) \vee (V_{out} \leq V_{0.1} + 0.001 \times V_{dd})]) \wedge \neg((V_{in} > (V_{dd} - V_{tp})) \vee (V_{in} \leq (V_{dd} - V_{tp})))$

The output of CMOS NOR2 for the input $V_{inA} = V_{inB}$= 0→1 is shown in Figure 6.3a in chapter 6.

3.5.2 Case 2 : $V_{inA} = 0$, $V_{inB} = 0 \rightarrow 1$

As input V_{inA} is low, so, pMOS P_1 is always in triode state and nMOS N_1 is always in cut-off state. The operation of the CMOS NOR2 is found to progress through the following regions for input V_{inB} switching from 0→1. For case 2, the initial location is *sA*.

Region A: Here ⟨ pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Cut-off,

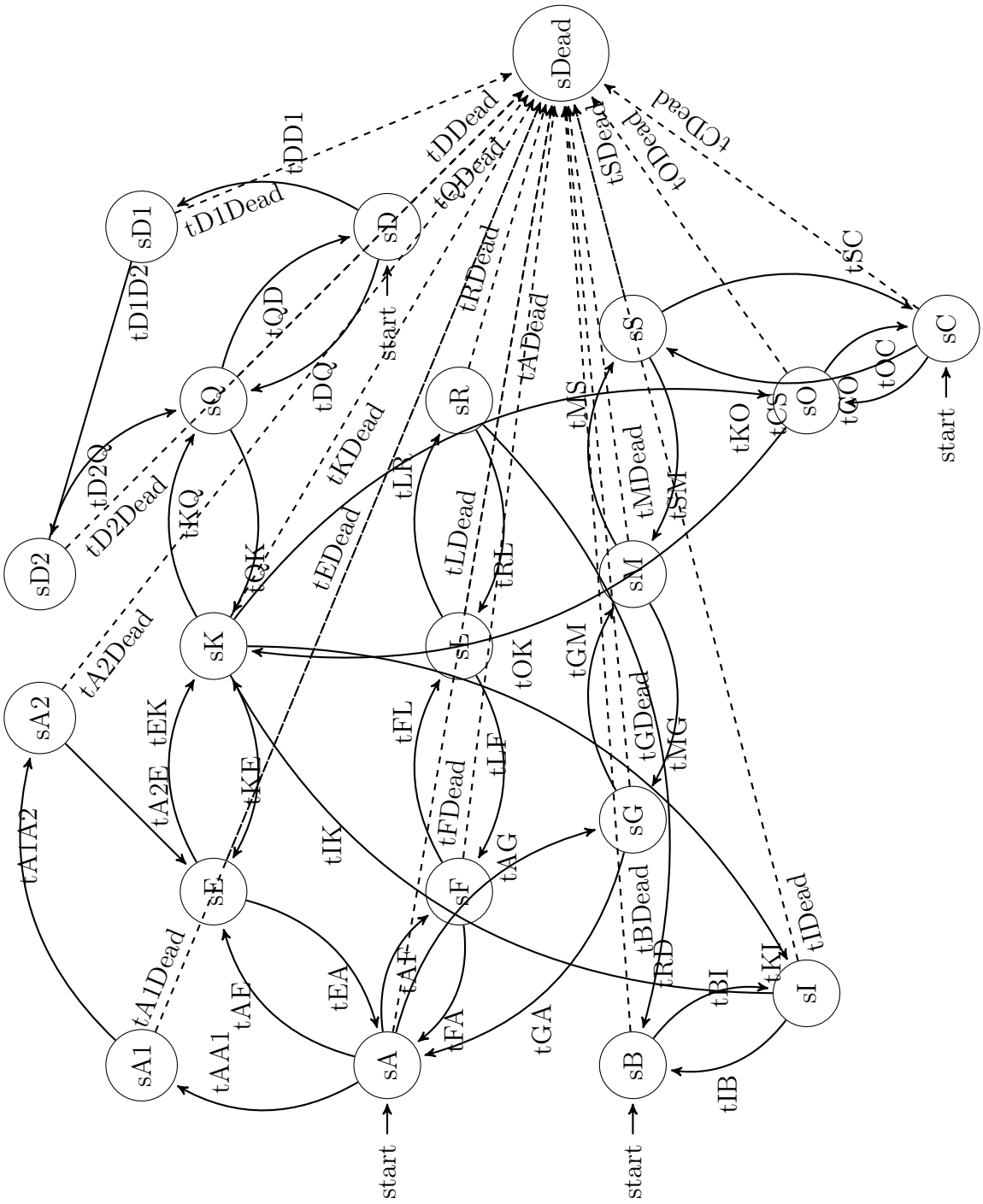


Figure 3.11: Stateflow model of CMOS NOR2.

nMOS N_2: Cut-off $\rangle$
Invariant : $(V_{\text{inB}} < V_{\text{tn}}) \wedge (V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inA}} = 0)$
Only the pMOS is conducting to charge the load capacitor towards. Therefore the only way to leave this region is by increasing V_{inA} and V_{inB} above V_{tn}. Violating the invariant condition, transition to region F takes place.
Region F: Here $\langle$ pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Cut-off, nMOS N_2: Saturation $\rangle$
Invariant: $(V_{\text{inB}} > V_{\text{tn}}) \wedge (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatpb}}) \wedge (V_{\text{out}} \geq V_{\text{dsatnb}}) \wedge (V_{\text{inA}} = 0)$
If the invariant condition is not satisfied, this region is left and transition to region L or region A takes place.
Region L: Here $\langle$ pMOS P_1: Triode, pMOS P_2: Saturation, nMOS N_1: Cut-off, nMOS N_2: Saturation $\rangle$
Invariant : $(V_{\text{inB}} > V_{\text{tn}}) \wedge V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}} \wedge (V_{\text{out}} \geq V_{\text{dsatnb}}) \wedge (V_{\text{inA}} = 0)$
If the invariant condition violates, the region is left and transition to region R or region F takes place.
Region R: Here $\langle$ pMOS P_1: Triode, pMOS P_2: Saturation, nMOS N_1: Cut-off, nMOS N_2: Triode $\rangle$
Invariant : $(V_{\text{inB}} > V_{\text{tn}}) \wedge (V_{\text{out}} < V_{\text{dsatnb}}) \wedge (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{inA}} = 0)$
Violating the invariant condition, transition to region B or region L takes place.
Region B: Here $\langle$ pMOS P_1: Triode, pMOS P_2: Cut-off, nMOS N_1: Cut-off, nMOS N_2: Triode $\rangle$
Invariant : $(V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inB}} > V_{\text{tn}}) \wedge (V_{\text{inA}} = 0)$
The pMOS P_1 is in triode state and the pMOS P_2 is in the cutoff state. As nmOS transistors are in parallel and only one nMOS is conducting, the load capacitor is discharged to GND through nMOS N_2.
Region Dead: This region is reached if a transition from a legal region of the system to another legal region, as described above, is not possible.
Invariant:

Transition A to Dead (tADead): $\neg((V_{\text{inB}} < V_{\text{tn}}) \vee (V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} = 0)) \wedge \neg((V_{\text{inB}} > V_{\text{tn}}) \vee (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} = 0))$

Transition F to Dead (tFDead): $\neg((V_{\text{inB}} > V_{\text{tn}}) \vee (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatpb}}) \vee (V_{\text{out}} \geq V_{\text{dsatnb}}) \vee (V_{\text{inA}} = 0)) \wedge \neg((V_{\text{inB}} < V_{\text{tn}}) \vee (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatpb}}) \vee (V_{\text{out}} \leq V_{\text{dsatnb}}) \vee (V_{\text{inA}} = 0))$

Transition L to Dead (tLDead): $\neg((V_{\text{inB}} > V_{\text{tn}}) \vee V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}} \vee (V_{\text{out}} \geq V_{\text{dsatnb}}) \vee (V_{\text{inA}} = 0)) \wedge \neg((V_{\text{inB}} < V_{\text{tn}}) \vee V_{\text{dsatpb}} < V_{\text{out}} - V_{\text{dd}} \vee (V_{\text{out}} \leq V_{\text{dsatnb}}) \vee (V_{\text{inA}} = 0))$

Transition R to Dead (tRDead): $\neg((V_{\text{inB}} > V_{\text{tn}}) \vee (V_{\text{out}} < V_{\text{dsatnb}}) \vee (V_{\text{dsatpb}} >$

$V_{out} - V_{dd}) \vee (V_{inA} = 0) \wedge \neg((V_{inB} < V_{tn}) \vee (V_{out} > V_{dsatnb}) \vee (V_{dsatpb} < V_{out} - V_{dd}) \vee (V_{inA} = 0)$

Transition B to Dead (tBDead): $\neg((V_{inB} > V_{dd} - V_{tp}) \vee (V_{inB} > V_{tn}) \vee (V_{inA} = 0)) \wedge \neg((V_{inB} < V_{dd} - V_{tp}) \vee (V_{inB} < V_{tn}) \vee (V_{inA} = 0))$

The output of CMOS NOR2 for the input $V_{inA} = 0$ and the input $V_{inB} = 0 \rightarrow 1$ has been shown in figure 6.3c chapter 6.

3.5.3 Case 3: V_{inB} =0, V_{inA} =0→1

As input V_{inB} is low, so, pMOS P_2 is always in triode state and nMOS N_2 is always in cut-off state. The operation of the CMOS NOR2 is found to progress through the following regions for input V_{inA} switching from 0→1. For case 3, the initial location is *sA*.

Region A: Here ⟨ pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Cut-off, nMOS N_2: Cut-off ⟩

Invariant : $(V_{inA} < V_{tn}) \wedge (V_{inA} < V_{dd} - V_{tp}) \wedge (V_{inB} = 0)$

Only the pMOS is conducting to charge the load capacitor towards . Therefore the only way to leave this region is by increasing V_{inA} and V_{inB} above V_{tn}. Violating the invariant condition, transition to region G takes place.

Region G: Here ⟨ pMOS P_1: Triode, pMOS P_2: Triode, nMOS N_1: Saturation, nMOS N_2: Cut-off ⟩

Invariant: $(V_{inA} > V_{tn}) \wedge (V_{out} - V_{dd} \geq V_{dsatpa}) \wedge (V_{out} \geq V_{dsatna}) \wedge (V_{inB} = 0)$

If the invariant condition is not satisfied, this region is left and transition to region M or region A takes place.

Region M: Here ⟨ pMOS P_1: Saturation, pMOS P_2: Triode, nMOS N_1: Saturation, nMOS N_2: Cut-off ⟩

Invariant : $(V_{inA} > V_{tn}) \wedge V_{dsatpa} > V_{out} - V_{dd} \wedge (V_{out} \geq V_{dsatna}) \wedge (V_{inB} = 0)$

If the condition violates, the region is left and transition to region S or region G is made.

Region S: Here ⟨ pMOS P_1: Saturation, pMOS P_2: Triode, nMOS N_1: Triode, nMOS N_2: Cut-off ⟩

Invariant : $(V_{inA} > V_{tn}) \wedge (V_{out} < V_{dsatna}) \wedge (V_{dsatpa} > V_{out} - V_{dd}) \wedge (V_{inB} = 0)$

Violating the invariant condition, transition to region C or region M takes place.

Region C: Here ⟨ pMOS P_1:Cut-off, pMOS P_2: Triode, nMOS N_1: Triode, nMOS N_2: Cut-off ⟩

Invariant : $(V_{inA} > V_{dd} - V_{tp}) \wedge (V_{inA} > V_{tn}) \wedge (V_{inB} = V_{dd})$

The pMOS P_2 is in triode state and the pMOS P_1 is in the cutoff state. As nmOS transistors are in parallel and only one nMOS is conducting, the load capacitor is discharged to GND through nMOS N_1.

Region Dead: This region is reached if a transition from a legal region of the system to another legal region, as described above, is not possible.
Invariant:

Transition A to Dead (tADead): $\neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} = 0)) \wedge \neg((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} = 0))$

Transition G to Dead (tGDead): $\neg((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatpa}}) \vee (V_{\text{out}} \geq V_{\text{dsatna}}) \vee (V_{\text{inB}} = 0)) \wedge \neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatpa}}) \vee (V_{\text{out}} \leq V_{\text{dsatna}}) \vee (V_{\text{inB}} = 0))$

Transition M to Dead (tMDead): $\neg((V_{\text{inA}} > V_{\text{tn}}) \vee V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}} \vee (V_{\text{out}} \geq V_{\text{dsatna}}) \vee (V_{\text{inB}} = 0)) \wedge \neg((V_{\text{inA}} < V_{\text{tn}}) \vee V_{\text{dsatpa}} < V_{\text{out}} - V_{\text{dd}} \vee (V_{\text{out}} \leq V_{\text{dsatna}}) \vee (V_{\text{inB}} = 0))$

Transition S to Dead (tSDead): $\neg((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{out}} < V_{\text{dsatna}}) \vee (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{inB}} = 0)) \wedge \neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{out}} > V_{\text{dsatna}}) \vee (V_{\text{dsatpa}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{inB}} = 0))$

Transition C to Dead (tCDead): $\neg((V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{inB}} = V_{\text{dd}})) \wedge \neg((V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{inB}} = V_{\text{dd}}))$

The output of CMOS NOR2 for the input $V_{\text{inA}} = 0 \rightarrow 1$ and the input $V_{\text{inB}} = 0$ has been shown in figure 6.3b chapter 6.

3.5.4 Case 4 : V_{inA}=0→1, V_{inB}=1→0

The operation of the CMOS NOR2 is found to progress through the following regions for input V_{inA} switching from 0→1 and input V_{inB} switching from 1→0. For case 4, the initial location is *sB*.
Region B: Here ⟨ pMOS P_1: Triode, pMOS P_2: Cut-off, nMOS N_1: Cut-off, nMOS N_2: Triode ⟩
Invariant: $(V_{\text{inA}} < V_{\text{tn}}) \wedge (V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inB}} > V_{\text{tn}})$.
The only way to leave this region is by increasing V_{inA} above V_{tn}. Since only one pMOS is conducting, the load capacitor does not charged to V_{dd} through pMOS P_1. As nMOS transistors are in parallel and only one N_2 nMOS is conducting, the load capacitor is discharged to GND through nMOS N_2. If the invariant is violated, transition is made to region I.
Region I: Here ⟨ pMOS P_1: Triode, pMOS P_2: Saturation, nMOS N_1: Saturation, nMOS N_2: Triode ⟩.
Invariant: $(V_{\text{inA}} > V_{\text{tn}}) \wedge (V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{dsatpb}} < V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{out}} > V_{\text{dsatna}})$
If the invariant is violated, transition is made to region B or region K.

Region K: Here ⟨ pMOS P_1: Saturation, pMOS P_2: Saturation, nMOSN_1: Saturation, nMOS N_2: Saturation ⟩.
Invariant : $(V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}})$ and $(V_{\text{out}} > V_{\text{dsatna}}) \wedge (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}})$ and $(V_{\text{out}} > V_{\text{dsatnb}})$
If the invariant condition is not satisfied, transition to region O or region I takes place.
Region O: Here ⟨ pMOS P_1: Saturation, pMOS P_2: Triode, nMOS N_1: Triode, nMOS N_2: Saturation ⟩
Invariant : $((V_{\text{inA}} > V_{\text{tn}}) \wedge (V_{\text{out}} < V_{\text{dsatna}})) \wedge (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \wedge (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{out}} > V_{\text{dsatnb}})$
If the invariant condition is not satisfied, transition to region C or region K takes place.
Region C: ⟨ pMOS P_1: Cut-off, pMOS P_2: Triode, nMOS N_1: Triode, nMOS N_2: Cut-off ⟩.
Invariant : $(V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inB}} < V_{\text{tn}}) \wedge (V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \wedge (V_{\text{inA}} > V_{\text{tn}})$
The pMOS P_2 is in triode state and the pMOS P_1 is in the cutoff state. As nMOS transistors are in parallel and only one nMOS is conducting, the load capacitor is discharged to GND through nMOS N_1.
Region Dead: This region is reached if a transition from a legal region of the system to another legal region, as described above, is not possible.
Invariant:

Transition B to Dead (tBDead): $\neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} > V_{\text{tn}})) \wedge \neg((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} < V_{\text{tn}}))$

Transition I to Dead (tIDead): $\neg((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{inA}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{dsatpb}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} > V_{\text{dsatna}})) \wedge \neg((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} < V_{\text{dsatna}}))$

Transition K to Dead (tKDead): $\neg((V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} > V_{\text{dsatna}}) \vee (V_{\text{dsatpb}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} > V_{\text{dsatnb}})) \wedge \neg((V_{\text{dsatpa}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} < V_{\text{dsatna}}) \vee (V_{\text{dsatpb}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{out}} < V_{\text{dsatnb}}))$

Transition O to Dead (tODead): $\neg(((V_{\text{inA}} > V_{\text{tn}}) \vee (V_{\text{out}} < V_{\text{dsatna}})) \vee (V_{\text{dsatpa}} > V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{out}} > V_{\text{dsatnb}})) \wedge \neg(((V_{\text{inA}} < V_{\text{tn}}) \vee (V_{\text{out}} > V_{\text{dsatna}})) \vee (V_{\text{dsatpa}} < V_{\text{out}} - V_{\text{dd}}) \vee (V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{out}} < V_{\text{dsatnb}}))$

Transition C to Dead (tCDead): $\neg((V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} < V_{\text{tn}}) \vee (V_{\text{inB}} < V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} > V_{\text{tn}})) \wedge \neg((V_{\text{inA}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inB}} > V_{\text{tn}}) \vee (V_{\text{inB}} > V_{\text{dd}} - V_{\text{tp}}) \vee (V_{\text{inA}} < V_{\text{tn}}))$

The output of CMOS NOR2 for the input $V_{\text{inA}} = 0 \rightarrow 1$ and the input $V_{\text{inB}} = 1 \rightarrow 0$ as shown in Figure 6.3d has been shown in chapter 6.

3.6 Summary

In this chapter, the characteristics of the MOSFET models has been described, and also how to model a MOS transistor in a circuit description. The SPICE program has provided three built-in MOS transistor models. However, the Level-2 model has been considered, which contains expressions from detailed device physics and also considers second-order effects for small geometry transistors. The differential equation describing the CMOS circuits has been formulated to describe different operating regions of the transistors. For CMOS NAND2, transistor size of pMOS P1, P2 and nMOS N1, N2 are same to have equal conductivity. For CMOS NOR2, transistor size of pMOS P1, P2 and nMOS N1, N2 are same to have equal conductivity. As, the model has continuous states; variable-step continuous solver has been used. Thus, the stateflow model has been confirmed to be safe and an unwanted state is unreachable from the initial states.

Chapter 4

Modelling and Analysis of Transistor Operation using BSIM3v3 Level 49 MOSFET Model

The model described in the previous chapter consists modelling of simple CMOS circuits with few parameters which include the second order effects. Therefore, the work reported in this chapter has been extended to handle more complex combinational CMOS circuits modelled at a higher level, such as BSIM3v3 level 49.

This chapter is organized as follows. Section 4.1 presents transistor operation modelling followed by a description of MOSFET parameters and Level 49 model equations. Section 4.2 discusses the mechanism of precharge based circuit. Section 4.3 presents the Stateflow model of the secure circuit, which is based on top-bottom pre-charge logic. Finally, summary of the chapter is presented in Section 4.4.

4.1 Transistor Operation Modelling

BSIM3v3 is the standard MOSFET model for deep submicron digital and analog circuit designs. BSIM3v3 is based on Poisson's equation and coherent quasi 2D analysis [54]. In this work, the short-channel and small geometry effects are considered for the threshold voltage and mobility calculations [72] and drain-induced barrier lowering effect has been introduced. The accuracy of the model depends on the equations governing the behaviour of the MOSFETs and the influence of the various model parameters. So, in this chapter stateflow modelling of operation of complex CMOS transistor cir-

cuits at BSIM3v3 level 49 [73] has been carried out taking into account parasitic capacitances.

4.1.1 Description of MOSFET Parameters at Level 49

Non-Uniform Doping and Small Channel Effects on Threshold Voltage : BSIM3v3 considers the following physical phenomena observed in MOSFET devices :

- **Threshold Voltage** : Accurate modelling of threshold voltage (V_{th}) is one of the most important requirements for description of device electrical characteristics more precisely. For MOSFET's with long channel length/width and uniform substrate doping concentration, V_{to} is already explained in chapter 3

- **Vertical Non-Uniform Doping Effect** : Due to V_{th}, the substrate doping concentration is higher near the surface as compared to the substrate. When the channel length is short, narrow, or both, the substrate doping concentration is not uniform. Then the threshold voltage equation includes body effect coefficients. The first-order body effect coefficient (k_1) and second-order body effect coefficient (k_2)are calculated as

$$k_1 = \gamma_2 - 2 \cdot k_2 \cdot \sqrt{\phi_s - V_{bm}} \tag{4.1}$$

$$k_2 = (\gamma_1 - \gamma_2) \cdot \frac{\sqrt{\phi_s - V_{\text{bx}}} - \sqrt{\phi_s}}{2 \cdot \sqrt{\phi_s} \cdot (\sqrt{\phi_s - V_{\text{bm}}} - \sqrt{\phi_s}) + V_{\text{bm}}} \tag{4.2}$$

where, γ_1 is body effect coefficient near the surface, γ_2 is body effect coefficient in the bulk.

$V_{\text{bx}} = \phi_s - (\frac{\sqrt{q \cdot \text{nchannel} \cdot X_t^2}}{2 \cdot \epsilon_{si}})$

where, V_{bx} is the V_{bs} at which the depletion width equals X_t, V_{bm} is maximum substrate bias, X_t is doping depth, NSUB is substrate doping concentration, nchannel is peak doping concentration near the surface. γ_1, γ_2, V_{bx}, X_t are the process parameter.

This non-uniformity will make γ, a function of the substrate bias. If the depletion width is less than X_t, γ is calcuated using equation (4.3);

otherwise it is calcuated using equation (4.4).

$$\gamma_1 = \frac{\sqrt{2 \cdot q \cdot \epsilon_{\text{si}} \cdot \text{nchannel}}}{c_{\text{ox}}} \tag{4.3}$$

$$\gamma_2 = \frac{\sqrt{2 \cdot q \cdot \epsilon_{\text{si}} \cdot \text{NSUB}}}{c_{\text{ox}}} \tag{4.4}$$

where, NSUB is substrate doping concentration, nchannel is peak doping concentration near the surface.

- **Lateral Non-Uniform Doping Effect :** The doping concentration near the source or drain is higher than that in the middle of the channel. As the channel length becomes shorter, lateral non-uniform doping will cause V_{th} to increase.

$$N_{\text{eff}} = N_a \left(1 + \frac{\text{nlx}}{L_{\text{eff}}}\right) \tag{4.5}$$

where, nlx is lateral nonuniform doping along channel, N_a is the substrate doping concentration

- **Short Channel Effect :** A MOSFET is defined as a short-channel device if the effective channel length (L_{eff}) is approximately equal to the source and drain junction depth. The threshold voltage of a long channel device is independent of the channel length and the drain voltage. As the channel length becomes shorter, the threshold voltage depends on the channel length and the drain voltage.

$$\Delta V_{\text{th}} = \theta_{\text{th}} \cdot (V_{\text{bi}} - \phi_s) \tag{4.6}$$

where, $\theta_{\text{th}} = \text{dvt0} \cdot [exp(\frac{-\text{dvt1} \cdot l_{\text{eff}}}{2 \cdot lt}) + 2 \cdot exp(\frac{-\text{dvt1} \cdot l_{\text{eff}}}{lt})]$,
$lt = (\sqrt{(3 \cdot t_{\text{ox}} \cdot \text{xdep})}) \cdot (1 + \text{dvt2} \cdot V_{\text{bs}})$, $\text{xdep} = \sqrt{\frac{2 \cdot \epsilon_{\text{si}} \cdot (\phi_s - V_{\text{bs}})}{q \cdot \text{nchannel}}}$
where, xdep is the depletion width in the substrate, dvt0 is short-channel effect coefficient 0, dvt1 is short-channel effect coefficient 1, dvt2 is short-channel effect coefficient 2.

- **Narrow Channel Effect :** Considering the narrow channel effect that is the width of the devices are getting narrow. The change in V_{th} is

modeled by equation (4.7)

$$(k_3 + k_{3b} \cdot V_{bs}) \cdot \left(\frac{t_{ox}}{(w_{effn} + w0)} \right) \tag{4.7}$$

After considerations of the above physical phenomena i.e. non-uniform doping, short and narrow channel effects on threshold voltage, the final V_{th} is expressed in equation (4.12).

Mobility Model : Mobility depends on many process parameters and bias conditions. For example, mobility depends on the gate oxide thickness, substrate doping concentration etc. Mobility of carrier is calculated as

$$\mu_{eff} = \frac{\mu_0}{(1 + \mu_a \cdot \left(\frac{V_{gs}+V_{th}}{t_{ox}} \right) + \mu_b \cdot \left(\frac{V_{gs}+V_{th}}{t_{ox}} \right)^2 + (\mu_c \cdot V_{bs}))} \tag{4.8}$$

where, μ_0 is low field mobility, μ_a is first-order mobility degradation coefficient, μ_b is second-order mobility degradation coefficient and μ_c is body bias sensitivity coefficient of mobility.

Carrier Drift Velocity : The parameter E_{sat} is the critical electrical field at which the carrier velocity becomes saturated.

$$v = \begin{cases} \frac{\mu_{eff} E}{1+(\frac{E}{E_{sat}})}, & E < E_{sat} \\ v_{sat}, & E > E_{sat} \end{cases}$$

where, v_{sat} is saturation velocity of carrier, $E_{sat} = 2 \cdot \frac{v_{sat}}{\mu_{eff}}$.

Bulk Charge Effect : As the depletion thickness of the channel is non-uniform, thus causes V_{th} to vary along the channel. This effect is called bulk charge effect. The parameter, A_{bulk}, is used to take into account the bulk charge effect. However, different parameters such as a0 , b0 , b1 are introduced to consider the channel length and width dependencies of the bulk charge effect. The parameter keta is introduced to model the change in bulk charge effect under high substrate bias conditions. Considering for BULKMOD=1, A_{bulk} is calulated as

$$A_{bulk} = \frac{1 + \frac{k_1 \cdot a0 \cdot l_{eff}}{\left(l_{eff}+2 \cdot \sqrt{xj \cdot xdep}\right) \cdot \sqrt{\phi_s - V_{bs}} \cdot 2}}{(1 + \text{keta} \cdot V_{bs})} \tag{4.9}$$

where, a0 is bulk charge effect, keta is body-bias coefficient of bulk charge effect, xj is junction depth.

Channel Length Modulation : Based on the quasi-two dimensional approximation, V_{aclm} is calculated as

$$V_{\text{aclm}} = \frac{1}{\text{pclm}} \cdot \left(\frac{A_{\text{bulk}} \cdot E_{\text{sat}} \cdot l_{\text{eff}} + V_{\text{gst}}}{A_{\text{bulk}} \cdot E_{\text{sat}} \cdot \text{litl}} \right) \cdot (V_{\text{ds}} - V_{\text{dsat}}) \tag{4.10}$$

where, V_{aclm} is the Early Voltage due to channel length modulation, pclm is the coefficient of channel length modulation values for less than 0, litl = $\sqrt{\frac{\epsilon_{si} \cdot tox \cdot xj}{\epsilon_{ox}}}$

Drain-Induced Barrier Lowering (DIBL) : The Early voltage due to the DIBL effect can be calculated as:

$$V_{adibl} = \frac{1}{\text{thetarout}} \cdot \left[(V_{gs} - V_{th}) - \left(\frac{1}{A_{\text{bulk}} \cdot V_{dsat}} + \frac{1}{V_{gst}} \right)^{-1} \right] \tag{4.11}$$

thetarout is calculated as
thetarout = pdibl1 $\cdot \left[\exp\left(\frac{-drout \cdot l_{eff}}{2 \cdot lt} \right) + 2 \cdot \exp\left(\frac{-\text{drout} \cdot l_{eff}}{lt} \right) \right]$ + pdibl2

where, pdibl1 is drain induced barrier lowering effect coefficient 1, pdibl2 is drain induced barrier lowering effect coefficient 2, drout is the length dependence coefficient of the DIBL.

4.1.2 MOSFET Level 49 Model Equation

The threshold voltage equation for the BSIM3 Level 49 model is expressed as

$$\begin{aligned} V_{th} =& V_{\text{th0}} + k_1 \cdot (\sqrt{(\phi_s - V_{\text{bs}})} - \sqrt{(\phi_s)}) - k_2 \cdot V_{\text{bs}} + \\ & k_1 \cdot \left(\sqrt{1 + \frac{\text{nlx}}{l_{\text{eff}}} \cdot \sqrt{\frac{\phi_s}{(\phi_s - V_{\text{bs}})}}} - 1 \right) \cdot \sqrt{(\phi_s)} + \\ & (k_3 + k_{3\text{b}} \cdot V_{\text{bs}}) \cdot \left(\frac{t_{\text{ox}}}{(w_{\text{effn}} + w0)} \right) \cdot \phi_s - \Delta V_{\text{th}} \end{aligned} \tag{4.12}$$

where, V_{th0} is threshold voltage of long channel, ΔV_{th} is the threshold voltage reduction due to the short channel effect, k_1 is first-order body effect coefficient, k_2 is second-order body effect coefficient, k_3 is narrow width effect coefficient, $k_{3\text{b}}$ is body width coefficient of narrow width effect, nlx is lateral nonuniform doping along channel, t_{ox} is gate oxide thickness, $w0$ is narrow

width effect coefficient, $\phi_s = 2 \cdot V_{\text{tm}} \cdot \log\left(\frac{nchannel}{n_i}\right)$,

$V_{bi} = V_{\text{tm}} \cdot \log\left(\frac{(1e20) \cdot nchannel}{n_i^2}\right)$,

The saturation voltage is expressed as :

$$V_{\text{dsat}} = \frac{E_{\text{sat}} \cdot l_{\text{eff}} \cdot V_{\text{gst}}}{A_{\text{bulk}} \cdot E_{\text{sat}} \cdot l_{\text{eff}} \cdot V_{\text{gst}}} \tag{4.13}$$

where, $V_{\text{gst}} = V_{\text{gs}} - V_{\text{th}}$.

The drain current I_D, through nMOS transistor is given by three modes of operation (considering subthMod = 0).

a) Cut-off mode: When no drain current flows through the transistor i.e. $I_D = 0$ occurs when $V_{\text{gsn}} < V_{\text{thn}}$. Where, V_{gsn} is gate to source voltage , V_{tn} is threshold voltage.

b) Triode Mode: It is a linear region. It occurs when $V_{\text{gsn}} > V_{\text{thn}}$ and $V_{\text{dsn}} < V_{\text{dsatn}}$. The current equation (4.15) in triode mode is given as:

$$\begin{aligned} i_{\text{dslin0}} =& u_{\text{eff}} \cdot c_{\text{ox}} \cdot \frac{w_{\text{effn}}}{l_{\text{eff}}} \cdot \frac{1}{1 + \frac{V_{\text{dsn}}}{(E_{\text{sat}} \cdot L)}} \cdot \\ & (V_{\text{gsn}} - V_{\text{thn}} - A_{\text{bulk}} \cdot \frac{V_{\text{dsn}}}{2}) \cdot V_{\text{dsn}} \end{aligned} \tag{4.14}$$

$$i_{\text{ds}} = \frac{i_{\text{dslin0}}}{1 + \frac{R_{\text{dsn}} \cdot idslin0}{V_{\text{dsn}}}} \tag{4.15}$$

where, $c_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}$

c_{ox} is the gate oxide capacitor per unit area, ϵ_{ox} is dielectric constant of SiO_2, t_{ox} is the thickness of oxide layer, w_{eff} channel width, l_{eff} is effective channel length.

c) Saturation Mode: For a constant V_{gsn}, with the increase of drain to source voltage the channel gets pinched off at the drain, $V_{\text{dsn}} > V_{\text{dsatn}}$. The current equation (4.17) in saturation mode is given as:

$$i_{\text{dsat}} = w_{\text{effn}} \cdot v_{\text{satn}} \cdot c_{\text{ox}} \cdot (V_{\text{gsn}} - V_{\text{thn}} - (A_{\text{bulk}} \cdot V_{\text{dsatn}})) \cdot \text{pfactor} \tag{4.16}$$

where, pfactor = $(a1 \cdot V_{\text{gst}}) + a2$, a1 is first nonsaturation factor, a2 is second nonsaturation factor.

$$i_{\mathrm{ds}} = i_{\mathrm{dsat}} \cdot \left(1 + \frac{V_{\mathrm{dsn}} - V_{\mathrm{dsatn}}}{V_{\mathrm{a}}}\right) \cdot \left(1 + \frac{V_{\mathrm{dsn}} - V_{\mathrm{dsatn}}}{V_{\mathrm{ahce}}}\right) \tag{4.17}$$

where,

For early voltage, satmod=2

$$V_{\mathrm{a}} = V_{\mathrm{asat}} + \mathrm{fvag} \cdot \mathrm{uvds} \cdot \left(\frac{1}{V_{\mathrm{aclm}}} + \frac{1}{V_{\mathrm{adibl}}}\right)^{-1}$$

$$V_{\mathrm{ahce}} = \left[\frac{\mathrm{pscbe2}}{l_{\mathrm{eff}}} \cdot \exp\left(\frac{-\mathrm{pscbe1} \cdot \mathrm{litl}}{V_{\mathrm{ds}} - V_{\mathrm{dsat}}}\right)\right]^{-1}$$

$$V_{\mathrm{asat}} = \frac{E_{\mathrm{sat}} \cdot l_{\mathrm{eff}} + V_{dsat} + 2 \cdot R_{\mathrm{ds}} \cdot V_{\mathrm{satn}} \cdot cox \cdot w_{\mathrm{effn}} \cdot \left(V_{\mathrm{gst}} - \frac{A_{\mathrm{bulk}} \cdot V_{\mathrm{dsatn}}}{2}\right)}{2/\mathrm{pfactor} - 1 + R_{\mathrm{ds}} \cdot V_{\mathrm{satn}} \cdot cox \cdot w_{\mathrm{effn}} \cdot A_{\mathrm{bulk}}}$$

$R_{\mathrm{ds}} = R_{\mathrm{ds0}} + \frac{R_{\mathrm{dsw}}}{1e6 \cdot w_{\mathrm{effn}}}$, R_{ds0} is source drain contact resistance, R_{dsw} is source drain resistance per unit width,

$\mathrm{uvds} = 1 + \mathrm{eta} \cdot \frac{\mathrm{ldd}}{\mathrm{litl}}$, $\mathrm{fvag} = 1 + \frac{\mathrm{pvag} \cdot V_{\mathrm{gst}}}{E_{\mathrm{sat}} \cdot l_{\mathrm{eff}}}$, pvag is gate dependence of Early voltage.

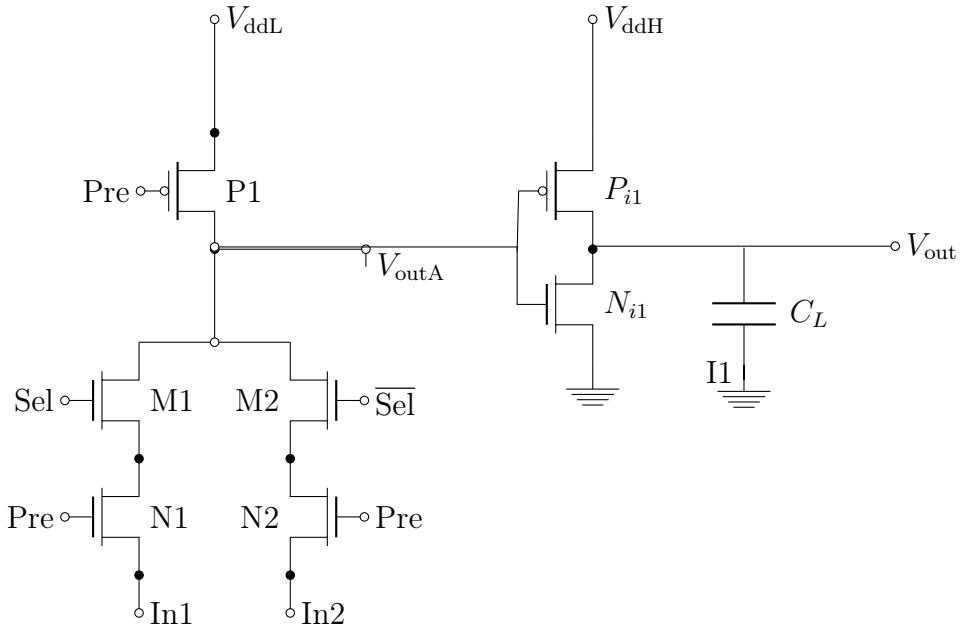
The differential equation describes the circuit operation of the dual rail precharge circuit.

$$\begin{aligned} &I_{\mathrm{n}} + C_{\mathrm{dbn}} \cdot \frac{\mathrm{d}V_{\mathrm{outA}}}{\mathrm{d}t} = I_{\mathrm{p}} - (C_{\mathrm{gdPi1}} + C_{\mathrm{gdNi1}}) \cdot \frac{\mathrm{d}V_{\mathrm{outA}}}{\mathrm{d}t} + \\ &(C_{\mathrm{gdn}} + C_{\mathrm{gdp}}) \cdot (\frac{\mathrm{d}V_{\mathrm{in}}}{\mathrm{d}t} - \frac{\mathrm{d}V_{\mathrm{outA}}}{\mathrm{d}t}) - C_{\mathrm{dbp}} \cdot \frac{\mathrm{d}V_{\mathrm{outA}}}{\mathrm{d}t} \end{aligned} \tag{4.18}$$

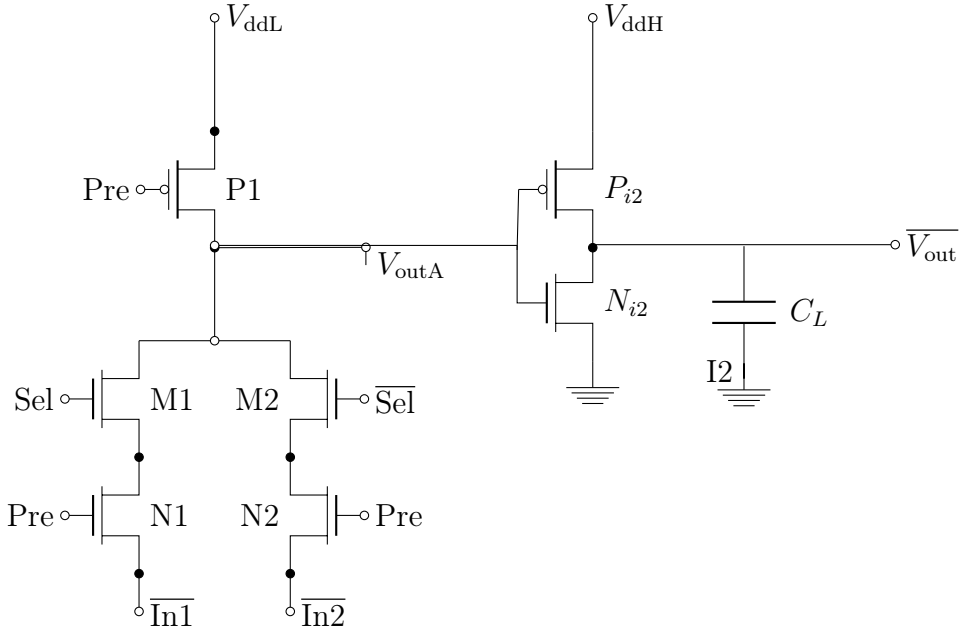
where, C_{L} is the load capacitance, C_{dbn}, C_{dbp} are the diffusion capacitances, C_{gdn}, C_{gdp} are the coupling capacitances, C_{gdPi1}, C_{gdNi1} are the coupling capacitances of CMOS inverter, V_{out} is the output voltage, I_{p} is the drain current through pMOS and I_{n} is the drain current through nMOS, V_{in} are the inputs (Pre or Sel) to the gate.

4.2 Mechanism of Dual-rail Precharge based Circuit

Precharging has been used to reduce the number of transistors in logic circuits and also to minimize the power dissipation of the circuit. It also helps to counter the skew in power dissipation of precharging free circuits when a long



(a) CMOS secure circuit 1



(b) CMOS secure circuit 2

Figure 4.1: Design of the basic cell with top-bottom precharge logic [74].

stream of logic 1 or logic 0 is produced in output. Precharge logic operates in two phases, namely, precharging phase and evaluation phase [75], [76]. In the design, logic has been used for the nNMOS (M1 and M2) circuitry, which is basically a multiplexer (MUX) in nature.

Top-Bottom Precharge Logic Configuration: It consists of a transistor pMOS (P1) along with an inverter (I1) connected to the top of the MUX and two nMOS transistors (N1 and N2) connected to the input nodes of the MUX as shown in Fig. 4.1. Depending on the select line of the MUX and the input parameters, different logic functions can be realized [77].

Pre-Charge Phase: We consider Fig. 4.1a precharge (Pre) is logic 0, the transistors N1 and N2 remain closed, so no input reaches the M1 and M2 transistor. However, the transistor P1 remains in an open state and thus the supply voltage V_{ddL} flows through the transistor and after inversion produces logic 0 at V_{out}. Thus, the output is always logic 0 (independent of the input value) when precharge is logic 0.

Evaluation Phase : When pre is logic 1, P1 remains closed while N1 and N2 remains open. Hence, the input signals flow through the M1 and M2 transistor reaches the inverter I1 and produces the inverted output. When Sel is logic 0, M1 remains closed while M2 remains open and thus, the input In2 flows through the transistor and produce the inverted output at V_{out}. Similarly, when Sel is logic 1, M2 remains closed while M1 remains open and thus, the input In1 flows through the transistor and produces the inverted output at V_{out}. Since signal strength reduces during propagation, the V_{ddH} is connected to the inverter I1 to restore the signal strength at the time of output. Note that the circuit is driven by a lower supply voltage V_{ddL} when Pre is logic 0, thus reducing the total power requirement of the circuit. The complementary circuit Fig. 4.1b operates in a similar manner.

4.3 Stateflow Model of Secure Circuit

The Stateflow model of the secure circuit has nighteen locations: sA, sB, sC, sD, sE, sF, sG, sH, sI, sJ, sK, sL, sM, sN, sO, sP, sQ, sR, sDead. Among these location, the Stateflow model is considered to be safe if the dead state (sdead) is unreachable from the initial states [71]. The operating regions of pMOS and nMOS transistors have been summarized in Table 4.1.

4.3.1 Choice of start state

Depending upon the input, the model have four different initial locations as *sA*, *sE*, *sI* and *sJ*. For input Pre=0→1 and Sel=0, the initial location is *sA*.

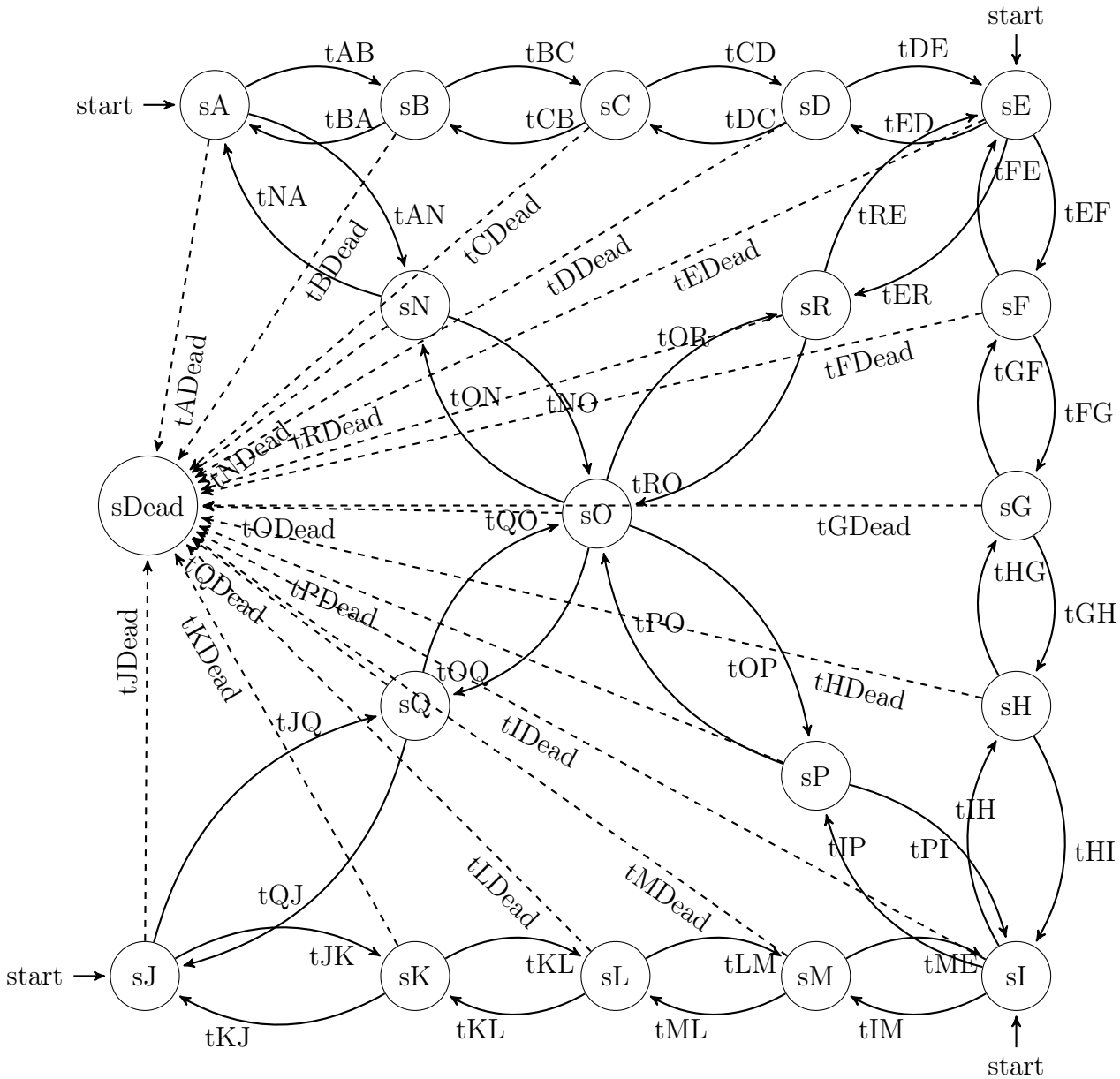


Figure 4.2: Stateflow model of secure circuit 1.

Region	pMOS state	nMOS state		nMOS state	
	P1	M1	M2	N1	N2
A	Triode	Cut-off	Triode	Cut-off	Cut-off
B	Triode	Cut-off	Triode	Saturation	Saturation
C	Saturation	Cut-off	Triode	Saturation	Saturation
D	Saturation	Cut-off	Triode	Triode	Triode
E	Cut-off	Cut-off	Triode	Triode	Triode
F	Cut-off	Saturation	Triode	Triode	Triode
G	Cut-off	Saturation	Saturation	Triode	Triode
H	Cut-off	Triode	Saturation	Triode	Triode
I	Cut-off	Triode	Cut-off	Triode	Triode
J	Triode	Triode	Cut-off	Cut-off	Cut-off
K	Triode	Triode	Cut-off	Saturation	Saturation
L	Saturation	Triode	Cut-off	Saturation	Saturation
M	Saturation	Triode	Cut-off	Triode	Triode
N	Triode	Saturation	Triode	Saturattion	Saturation
O	Saturation	Saturation	Saturation	Saturation	Saturation
P	Saturation	Triode	Saturation	Triode	Triode
Q	Triode	Triode	Saturation	Saturation	Saturation
R	Saturation	Triode	Saturation	Triode	Triode
Dead	-	-	-	-	-

Table 4.1: Operating regions of pMOS and nMOS transistors of secure circuit

⟨pMOS (P1): Triode, nMOS (M2): Triode, nMOS (M1, N1, N2): Cut-off⟩ As, Pre is the input to the pMOS P1 and nMOS N1, N2; Sel is the input to the M1; pMOS is conducting and nMOS transistors are not conducting.
For input Pre=0→1→1 and Sel= 1, the initial location is *sJ*. ⟨pMOS (P1): Triode, nMOS (M1): Triode, nMOS(M2, N1, N2): Cut-off⟩ As, Pre is the input to the pMOS P1 and nMOS N1, N2; Sel is the input to the M1; pMOS is conducting and nMOS transistors N1 and N2 are not conducting where as M1 is conducting.
For input Pre=1 and Sel=0→1, the initial location is *sE*. ⟨pMOS (P1): Cut-off, nMOS (M1): Cut-off, nMOS(M2, N1, N2): Triode⟩ As, Pre is the input to the pMOS P1 and nMOS N1, N2; Sel is the input to the M1; pMOS is not conducting and nMOS transistors N1 and N2 are conducting where as M1 is not conducting and M2 is conducting. For input Pre=1 and Sel=1→0, the initial location is *sI*.
⟨pMOS (P1): Cut-off, nMOS (M1): Triode, nMOS(M2): Cut-off , nMOS (N1, N2): Triode⟩ As, Pre is the input to the pMOS P1 and nMOS N1, N2; Sel is the input to the M1; pMOS is not conducting and nMOS transistors N1 and N2 are conducting where as M1 is conducting and M2 is not conducting.

The Stateflow model of secure circuit is shown in Figure 4.2. Here, as the input voltage is less than the threshold voltage, the initial location is sA, where the secure circuit remains for T1 time. The operation of the secure circuit is explained by applying logic 0 and logic 1 input, (Pre=011 and Sel=001) where the behaviour is characterised through the following sequence of regions.
Region A:⟨pMOS (P1): Triode, nMOS (M2): Triode, nMOS (M1, N1, N2): Cut-off⟩
Invariant: $(\mathrm{Pre} = 0 \wedge \mathrm{Pre} < V_{\mathrm{thn}}) \wedge \mathrm{Sel} = 0$
(Pre is the input to the pMOS P1, and Sel is the input to the M1, V_{thn} is the threshold voltage of nMOS transistor). Only the pMOS is conducting to charge the load capacitor towards V_{ddL}. When Pre increases so that $\mathrm{Pre} = V_{\mathrm{thn}}$ a transition occurs to region B

$$I_{\mathrm{p}} - C_{\mathrm{dbp}} \cdot \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} + (C_{\mathrm{gdp}}) \cdot \left(\frac{\mathrm{d}V_{\mathrm{in}}}{\mathrm{d}t} - \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} \right) = C_{\mathrm{L}} \cdot \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} \tag{4.19}$$

Region B: ⟨pMOS: Triode, nMOS (M1):Cut-off , nMOS (M2): Triode ,nMOS (N1, N2): Saturation ⟩
Invariant: $\mathrm{Pre} \geq V_{\mathrm{thn}} \wedge (V_{\mathrm{out}} - V_{\mathrm{dd}} \geq V_{\mathrm{dsatp}}) \wedge (V_{\mathrm{out}} \geq V_{\mathrm{dsatn}}) \wedge \mathrm{Sel} = 0.$
If the invariant conditon is not satisfied, this region is left and transition to region C takes place.
Region C: ⟨pMOS: Saturation, nMOS (M1):Cut-off , nMOS (M2): Triode

,nMOS (N1, N2): Saturation ⟩
Invariant: $(\text{Pre} \geq V_{\text{thn}}) \wedge (V_{\text{out}} \geq V_{\text{dsatn}}) \wedge (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}}) \wedge \text{Sel} = 0$.
If the condition violates, the region is left and transition to region D takes place.
Region D: ⟨pMOS: Saturation, nMOS (M1):Cut-off , nMOS (M2): Triode ,nMOS (N1, N2): Triode ⟩.
Invariant: $(\text{Pre} \geq V_{\text{thn}}) \wedge (V_{\text{out}} \leq V_{\text{dsatn}}) \wedge (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}}) \wedge \text{Sel} = 0$.
Violating the invariant condition, transition to region E takes place causing pMOS to enter its cutoff state.
Region E:⟨pMOS (P1): Cut-off, nMOS (M1): Cut-off, nMOS(M2, N1, N2): Triode⟩
Invariant: $(\text{Pre} \geq V_{\text{dd}} - V_{\text{thp}} \wedge \text{Pre} = V_{\text{dd}}) \wedge (V_{\text{out}} \leq V_{\text{dsatn}}) \wedge (\text{Sel} = 0)$
(Pre is the input to the nMOS N1 and N2, and Sel is the input to the M1, V_{thp} is the threshold voltage of pMOS transistor). Sel is logic 0, while nMOS transistor M1 is closed, nMOS transistor M2 remains open as $\overline{\text{Sel}}$ is logic 1; nMOS transistor (N1 and N2) do conduct as Pre is logic 1, thus the input In2 flows through the transistor. When Sel increases so that Sel = V_{thn} a transition occurs to region F

$$(I_{\text{nM2}} + I_{\text{nN2}}) + C_{\text{dbn}} \cdot \frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}t} = (C_{\text{gdn}}) \cdot \left(\frac{\mathrm{d}V_{\text{in}}}{\mathrm{d}t} - \frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}t} \right) - C_{\text{L}} \cdot \frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}t} \quad (4.20)$$

where, $C_{\text{dbn}} = C_{\text{dbnM2}} + C_{\text{dbnN2}}$ $C_{\text{gdn}} = C_{\text{gdnM2}} C_{\text{gdnN2}}$
Region F:⟨pMOS (P1): Cut-off, nMOS (M1): Saturation, nMOS (M2): Triode, nMOS(N1, N2): Triode⟩
Invariant: $\text{Pre} = V_{\text{dd}} \wedge (V_{\text{out}} \leq V_{\text{dsatn}} \wedge \text{Sel} \geq V_{\text{thn}} \wedge \overline{\text{Sel}} \leq V_{\text{dd}} - V_{\text{thp}})$.
If the invariant condition is not satisfied, this region is left and transition to region G takes place.
Region G:⟨pMOS (P1): Cut-off, nMOS (M1): Saturation, nMOS (M2): Saturation, nMOS(M2, N1, N2): Triode⟩
Invariant: $\text{Pre} = V_{\text{dd}} \wedge (V_{\text{out}} \geq V_{\text{dsatn}} \wedge \text{Sel} \geq V_{\text{thn}})$.
Violating the invariant condition, transition to region H takes place.
Region H:⟨pMOS (P1): Cut-off, nMOS (M1): Triode, nMOS (M2): Saturation, nMOS(M2, N1, N2): Triode⟩
Invariant: $\text{Pre} = V_{\text{dd}} \wedge (V_{\text{out}} \leq V_{\text{dsatn}} \wedge \overline{\text{Sel}} > V_{\text{thn}}) \wedge (\text{Sel} \geq V_{\text{thn}})$.
If the condition violates, the region is left and transition to region I takes place.
Region I:⟨pMOS (P1): Cut-off, nMOS (M1): Triode, nMOS(M2): Cut-off, nMOS(N1, N2): Triode⟩
Invariant:$\text{Pre} = V_{\text{dd}} \wedge (\text{Sel} \geq V_{\text{dd}} - V_{\text{thp}}) \wedge \text{Sel} = V_{\text{dd}}) \wedge (\overline{\text{Sel}} < V_{\text{thn}} \wedge \overline{\text{Sel}} = 0)$
(Pre is the input to the nMOS N1 and N2, and Sel is the input to the M1).

Sel is logic 1, while nMOS transistor M1 remains open, nMOS transistor M2 remains closed as $\overline{\text{Sel}}$ is logic 0; nMOS transistor (N1 and N2) do conduct as Pre is logic 1, thus the input In1 flows through the transistor.

$$(I_{\text{nM1}} + I_{\text{nN1}}) + C_{\text{dbn}} \cdot \frac{\text{d}V_{\text{out}}}{\text{d}t} = (C_{\text{gdn}}) \cdot \left(\frac{\text{d}V_{\text{in}}}{\text{d}t} - \frac{\text{d}V_{\text{out}}}{\text{d}t} \right) - C_{\text{L}} \cdot \frac{\text{d}V_{\text{out}}}{\text{d}t} \quad (4.21)$$

where, $C_{\text{dbn}} = C_{\text{dbnM1}} + C_{\text{dbnN1}}$, $C_{\text{gdn}} = C_{\text{gdnM1}} C_{\text{gdnN1}}$

Region Dead: This region is reached if a transition from a legal region of the system to another legal region, as described above, is not possible.
Invariant:

Transition A to Dead (tADead): $\neg((\text{Pre} = 0 \vee \text{Pre} > V_{\text{thn}}) \vee \text{Sel} = 0) \wedge \neg((\text{Pre} = 0 \vee \text{Pre} > V_{\text{thn}}) \vee \text{Sel} = 0)$

Transition B to Dead (tBDead): $\neg(\text{Pre} \geq V_{\text{thn}} \vee (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatp}}) \vee (V_{\text{out}} \geq V_{\text{dsatn}}) \vee \text{Sel} = 0) \wedge \neg(\text{Pre} \leq V_{\text{thn}} \vee (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}}) \vee (V_{\text{out}} \leq V_{\text{dsatn}}) \vee \text{Sel} = 0)$

Transition C to Dead (tCDead): $\neg((\text{Pre} \geq V_{\text{thn}}) \vee (V_{\text{out}} \geq V_{\text{dsatn}}) \vee (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}}) \vee \text{Sel} = 0) \wedge \neg((\text{Pre} \leq V_{\text{thn}}) \vee (V_{\text{out}} \leq V_{\text{dsatn}}) \vee (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatp}}) \vee \text{Sel} = 0)$

Transition D to Dead (tDDead): $\neg((\text{Pre} \geq V_{\text{thn}}) \vee (V_{\text{out}} \leq V_{\text{dsatn}}) \vee (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}}) \vee \text{Sel} = 0) \wedge \neg((\text{Pre} \leq V_{\text{thn}}) \vee (V_{\text{out}} \leq V_{\text{dsatn}}) \vee (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}}) \vee \text{Sel} = 0)$

Transition E to Dead (tEDead): $\neg((\text{Pre} \geq V_{\text{dd}} - V_{\text{thp}} \vee \text{Pre} = V_{\text{dd}}) \vee (V_{\text{out}} \leq V_{\text{dsatn}}) \vee (\text{Sel} = 0)) \wedge \neg((\text{Pre} \leq V_{\text{dd}} - V_{\text{thp}} \vee \text{Pre} = V_{\text{dd}}) \vee (V_{\text{out}} \geq V_{\text{dsatn}}) \vee (\text{Sel} = 0))$

Transition F to Dead (tFDead): $\neg(\text{Pre} = V_{\text{dd}} \vee (V_{\text{out}} \leq V_{\text{dsatn}} \vee \text{Sel} \geq V_{\text{thn}} \vee \overline{\text{Sel}} \leq V_{\text{dd}} - V_{\text{thp}})) \wedge \neg(\text{Pre} = V_{\text{dd}} \vee (V_{\text{out}} \geq V_{\text{dsatn}} \vee \text{Sel} \leq V_{\text{thn}} \vee \overline{\text{Sel}} \geq V_{\text{dd}} - V_{\text{thp}}))$

Transition G to Dead (tGDead): $\neg(\text{Pre} = V_{\text{dd}} \vee (V_{\text{out}} \geq V_{\text{dsatn}} \vee \text{Sel} \geq V_{\text{thn}})) \wedge \neg(\text{Pre} = V_{\text{dd}} \vee (V_{\text{out}} \leq V_{\text{dsatn}} \vee \text{Sel} \leq V_{\text{thn}}))$

Transition H to Dead (tHDead): $\neg(\text{Pre} = V_{\text{dd}} \vee (V_{\text{out}} \leq V_{\text{dsatn}} \vee \overline{\text{Sel}} > V_{\text{thn}}) \vee (Sel \geq V_{\text{thn}})) \wedge \neg(\text{Pre} = V_{\text{dd}} \vee (V_{\text{out}} \geq V_{\text{dsatn}} \vee \overline{\text{Sel}} < V_{\text{thn}}) \vee (\text{Sel} \leq V_{\text{thn}}))$

Transition I to Dead (tIDead): $\neg(\text{Pre} = V_{\text{dd}} \vee (\text{Sel} \geq V_{\text{dd}} - V_{\text{thp}}) \vee \text{Sel} == \text{logic 1}) \vee (\overline{\text{Sel}} < V_{\text{thn}} \vee \overline{\text{Sel}} = 0)) \wedge \neg(\text{Pre} = V_{\text{dd}} \vee (\text{Sel} \leq V_{\text{dd}} - V_{\text{thp}}) \vee \text{Sel} = V_{\text{dd}}) \vee (\overline{\text{Sel}} > V_{\text{thn}} \vee \overline{\text{Sel}} = 0))$

Similarly, the operation of the secure circuit is explained by applying Pre=011 and Sel= logic 1, where the behaviour is characterised through the following sequence of regions.
Region J:⟨pMOS (P1): Triode, nMOS (M1): Triode, nMOS(M2, N1, N2): Cut-off⟩
Invariant: $(\text{Pre} = 0 \wedge \text{Pre} < V_{\text{thn}}) \wedge \text{Sel} = V_{\text{dd}}$
(Pre is the input to the pMOS P1, and Sel is the input to the M1). Sel is logic 1, while nMOS transistor M1 is open and nMOS transistor (N1 and N2) does not conduct as Pre is logic 0, thus the input In1 does not flows through the transistor. Only the pMOS is conducting to charge the load capacitor towards V_{ddL}. When Pre increases so that $\text{Pre} = V_{\text{thn}}$ a transition occurs to region K
Region K: ⟨pMOS: Triode, nMOS (M1):Triode , nMOS (M2): Cut-off ,nMOS (N1, N2): Saturation ⟩
Invariant: $\text{Pre} \geq V_{\text{thn}} \wedge (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatp}}) \wedge (V_{\text{out}} \geq V_{\text{dsatn}}) \wedge \text{Sel} = V_{\text{dd}}$.
If the invariant conditon is not satisfied, this region is left and transition to region L takes place.
Region L: ⟨pMOS: Saturation, nMOS (M1):Triode , nMOS (M2): Cut-off ,nMOS (N1, N2): Saturation ⟩
Invariant: $(\text{Pre} \geq V_{\text{thn}}) \wedge (V_{\text{out}} \geq V_{\text{dsatn}}) \wedge (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}}) \wedge \text{Sel} = V_{\text{dd}}$.
If the condition violates, the region is left and transition to region M takes place.
Region M: ⟨pMOS: Saturation, nMOS (M1):Triode , nMOS (M2): Cut-off ,nMOS (N1, N2): Triode ⟩.
Invariant: $(\text{Pre} \geq V_{\text{thn}}) \wedge (V_{\text{out}} \leq V_{\text{dsatn}}) \wedge (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}}) \wedge \text{Sel} = V_{\text{dd}}$.
Violating the invariant condition, transition to region I takes place causing pMOS to enter its cutoff state.
Region I:⟨pMOS (P1): Cut-off, nMOS (M1): Triode, nMOS(M2): Cut-off, nMOS(N1, N2): Triode⟩
Invariant:$\text{Pre} = V_{\text{dd}} \wedge (\text{Sel} \geq V_{\text{dd}} - V_{\text{thp}}) \wedge \text{Sel} = V_{\text{dd}}) \wedge (\overline{\text{Sel}} < V_{\text{thn}} \wedge \overline{\text{Sel}} = 0)$
(Pre is the input to the nMOS N1 and N2, and Sel is the input to the M1). Sel is logic 1, while nMOS transistor M1 remains open, nMOS transistor M2 remains closed as $\overline{\text{Sel}}$ is logic 0; nMOS transistor (N1 and N2) do conduct as Pre is logic 1, thus the input In1 flows through the transistor.
Region Dead: This region is reached if a transition from a legal region of the system to another legal region, as described above, is not possible.
Invariant:

Transition J to Dead (tJDead): $\neg((\text{Pre} = 0 \vee \text{Pre} < V_{\text{thn}}) \vee \text{Sel} = V_{\text{dd}}) \wedge \neg((\text{Pre} = 0 \vee \text{Pre} > V_{\text{thn}}) \vee \text{Sel} = V_{\text{dd}})$

Transition K to Dead (tKDead): $\neg(\text{Pre} \geq V_{\text{thn}} \vee (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatp}}) \vee$

$(V_{\text{out}} \geq V_{\text{dsatn}}) \vee \text{Sel} = V_{\text{dd}}) \wedge (\neg \text{Pre} \leq V_{\text{thn}} \vee (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}}) \vee (V_{\text{out}} \leq V_{\text{dsatn}}) \vee \text{Sel} = V_{\text{dd}})$

Transition L to Dead (tLDead): $\neg((\text{Pre} \geq V_{\text{thn}}) \vee (V_{\text{out}} \geq V_{\text{dsatn}}) \vee (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}}) \vee \text{Sel} = V_{\text{dd}}) \wedge \neg((\text{Pre} \leq V_{\text{thn}}) \vee (V_{\text{out}} \leq V_{\text{dsatn}}) \vee (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatp}}) \vee \text{Sel} = V_{\text{dd}})$

Transition M to Dead (tMDead): $\neg((\text{Pre} \geq V_{\text{thn}}) \vee (V_{\text{out}} \leq V_{\text{dsatn}}) \vee (V_{\text{out}} - V_{\text{dd}} \leq V_{\text{dsatp}}) \vee \text{Sel} = V_{\text{dd}}) \wedge \neg((\text{Pre} \leq V_{\text{thn}}) \vee (V_{\text{out}} \geq V_{\text{dsatn}}) \vee (V_{\text{out}} - V_{\text{dd}} \geq V_{\text{dsatp}}) \vee \text{Sel} = V_{\text{dd}})$

Transition I to Dead (tIDead): $\neg(\text{Pre} = V_{\text{dd}} \vee (\text{Sel} \geq V_{\text{dd}} - V_{\text{thp}}) \vee \text{Sel} = V_{\text{dd}}) \vee (\overline{\text{Sel}} < V_{\text{thn}} \vee \overline{\text{Sel}} = 0)) \wedge \neg(\text{Pre} = V_{\text{dd}} \vee (\text{Sel} \leq V_{\text{dd}} - V_{\text{thp}}) \vee \text{Sel} = V_{\text{dd}}) \vee (\overline{\text{Sel}} > V_{\text{thn}} \vee \overline{\text{Sel}} = 0))$

4.4 Summary

In this chapter, the characteristics of the MOSFET models using higher level current equations have been described. The Berkeley Short-Channel IGFET Model (or BSIM in short) provides a analytically simple model but is based on a small number of parameters, which are normally extracted from experimental data. The BSIM3v3 model is used for modelling, ensuring that the important deep submicron effects are considered while optimising the transistor size. The differential equation describing the CMOS secure circuits has been formulated to describe different operating regions of the transistors. As, the model has continuous states; variable-step continuous solver has been used. Thus, the completeness of the model has been confirmed and in addition, it has been confirmed that the unwanted state is unreachable from the initial states.

Chapter 5

Parameter Optimisation for Delay and Power

The model described in the earlier chapter has a number of design parameters that must be determined for proper identification of the CMOS circuit behavior. The parameters should be identified so that requisite performance requirements such as minimisation of rise time, fall time and average power dissipation are met. In this chapter, STL properties are used in conjunction with the Breach tool in Matlab Simulink [17] to determine the parameters of the model for the various gates (CMOS inverter, CMOS NAND2 and CMOS NOR2) and dual-rail precharge circuit.

5.1 Signal Temporal Logic (STL)

Breach is a tool in Matlab Simulink that can interact with a Simulink model (stateflow model) by *i*) Changing the parameters of the model defined in the base workspace of Matlab, *ii*) Generating input signals, *iii*) Running simulations and collecting signals for analysis. Signal Temporal Logic (STL) is a formalism for reasoning about temporal properties of continuous-time traces of hybrid systems. An STL formula φ can be formulated for a signal x which can check whether the signal x satisfies the STL formula φ by computing the satisfaction signals [78] [79]. Breach works on STL properties [17] for a given Stateflow model and returns *false* (0), if no satisfying trace can be found; otherwise, *true* (1) is returned.The Breach model is shown in figure 5.1. Given a stateflow model M producing simulation traces t $\mapsto$ w[t], Breach can solve various problems involving optimisation of model parameters and specification φ expressed in STL. An execution trace w is a set of real-valued signals $x = (x_1, x_2..., x_n)$ defined over some interval D of $\mathbb{R}^+$, which is called

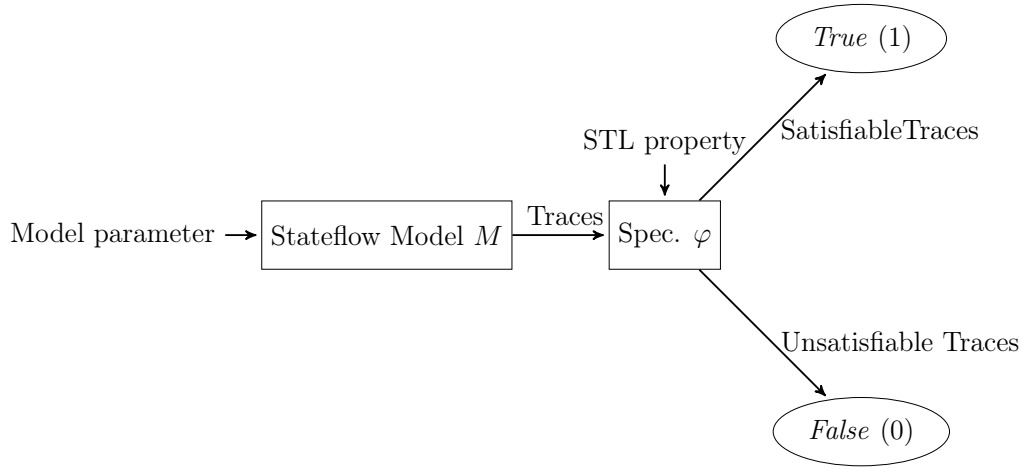


Figure 5.1: Breach model.

the time domain of w. The syntax of STL [80] is given as follows:

$$\varphi := true | x_i \geq 0 | \neg\varphi | \varphi \wedge \varphi | \varphi U_I \varphi$$

where, x_i are variables, and I is a closed, non-singular interval of $\mathbb{R}^+$. This includes bounded intervals $[a, b]$ and unbounded intervals $[a, +\infty)$ for any $0 \geq a < b$. Let w be a trace of time domain D.

Boolean Semantics For a trace w, the validity of an STL formula φ at a given time $t \in dom(\varphi, w)$ is set according to the following inductive definition.

- $(w, t) \vDash true$
- $(w, t) \vDash x_i \geq 0$ iff $x_i^w(t) \geq 0$
- $(w, t) \vDash \neg\varphi$ iff $(w, t) \nvDash \varphi$
- $(w, t) \vDash \varphi \wedge \psi$ iff $(w, t) \vDash \varphi \wedge (w, t) \vDash \psi$

5.2 Optimization Algorithm

5.2.1 Proposed 2D Search Algorithm

a) **Computation of rise time and fall time**

The rise time and fall times are computed by applying a steep ramp as input to the CMOS inverter. The rise and fall times of the ramp should be chosen to be negligile compared to the fall time and the rise time, respectively, of the CMOS inverter. From (5.1) that describes the circuit operation of the CMOS inverter we can say (for a given w_n):

$$\text{risetime}|_{\text{w}_\text{n}} \propto \frac{1}{\text{w}_\text{p}} \tag{5.1}$$

To compute rise time (t_r) of the output voltage, the output load ca-

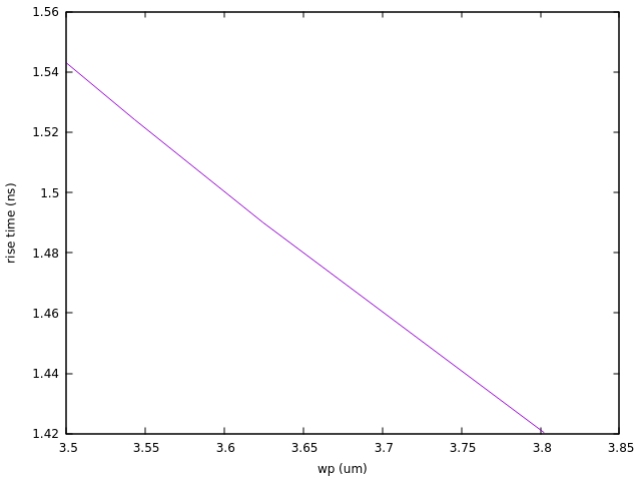


Figure 5.2: pMOS transistor width (μm) vs rise time (ns) of CMOS inverter for given nMOS transistor width (μm).

pacitor (C_L) should be charged through the active pMOS transistor, considering nMOS transistor is in cut-off mode. This is captured entirely in region A. Accordingly, the rise time is determined by noting the time spent in moving from region A1 to A2. Similarly, to calculate fall time (t_f) of the output voltage, the output load capacitor (C_L) should be discharged through the active nMOS transistor, considering pMOS transistor is in cut-off mode. This is captured entirely in region E. Accordingly, the fall time is determined by noting the time spent moving from region E1 to E2. On similar lines from (5.1), it may be

noted:

$$\text{falltime}|_{\text{w}_\text{p}} \propto \frac{1}{\text{w}_\text{n}} \tag{5.2}$$

To determine the rise time and fall time, first a range of parameters

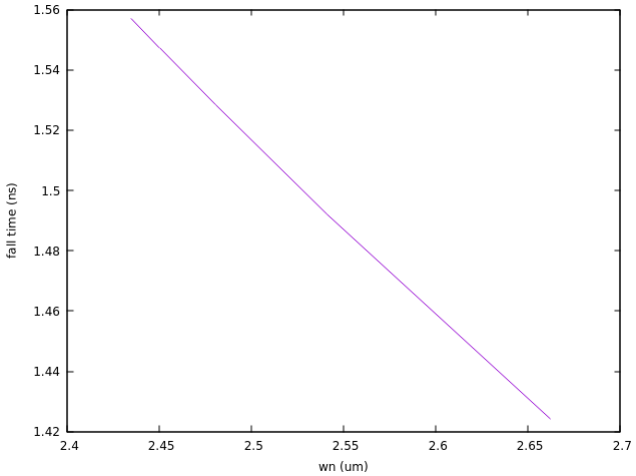


Figure 5.3: nMOS transistor width (μm) vs fall time (ns) of CMOS inverter for given pMOS transistor width (μm).

are found where the given model for the identified parameters satisfies the STL formula. The cmosBreach function applies the STL property to the given model. If the property is satisfied by the model, a positive value indicating success is returned. Otherwise, a negative value is returned indicating failure. The multiplying factor m0 should be greater than 1; here, m0=1.2 has been chosen for satisfactory step size as shown in Algorithm 1. A range is obtained from the given initial value of pMOS transistor width and nMOS transistor width, where p0 = 2.0 μm and n0 = 1.4 μm respectively. The range consists of two bounds, the lower bound (LB) and the upper bound (UB). The lower bound consists of nMOS and pMOS transistor width that satisfies the STL property, shown in Figure 5.4a. The upper bound consists of nMOS and pMOS transistor width that does not satisfy the STL property, shown in Figure 5.4b. From equation (5.2), fall time is inversely proportional to the nMOS transistor width for a given pMOS transistor width. Similarly, from equation (5.1), rise time is inversely proportional to the pMOS transistor width, for a given nMOS transistor width. With increase in nMOS transistor width and pMOS transistor width, fall time and rise time will decrease; Figure 5.3 and Figure 5.2

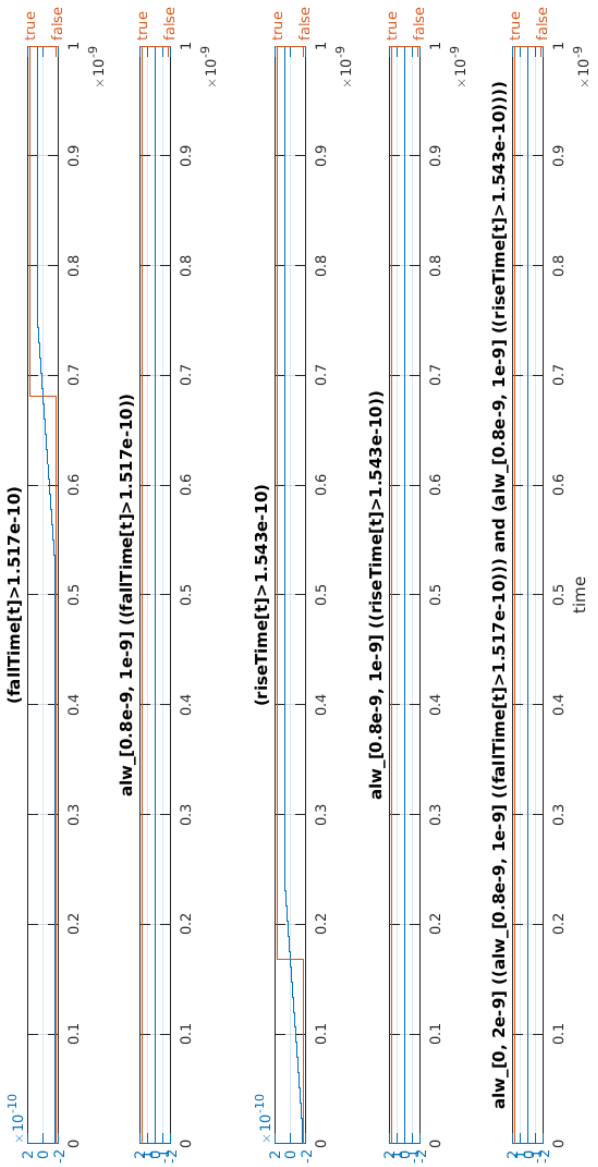
represent the same. So if the rise time and fall time decrease below min_tr and min_tf respectively (min_tr is the minimum rise time and min_tf is the minimum fall time that can be achieved), we get the upper bound value i.e. the first *false* value that does not satisfy the STL property, beyond which all values are *false* as shown in Figure 5.5. For the rise time and fall time above min_tr and min_tf respectively, we get the lower bound value i.e. the *true* value that satisfies the STL property, beyond which all values are *true*.

The STL property developed to capture the performance requirements at time t of CMOS inverter is described below.

```
param min_tr = 0.1543 e-9,
param min_tf = 0.1517 e-9
phitr_lw := riseTime[t] > min_tr
phitf_lw := fallTime[t] > min_tf
phi_ok := alw_[0.8e-9,1e-9] (phitr_lw and phitf_lw)
alw_phi := alw_[0, 1e-9](phi_ok)
```

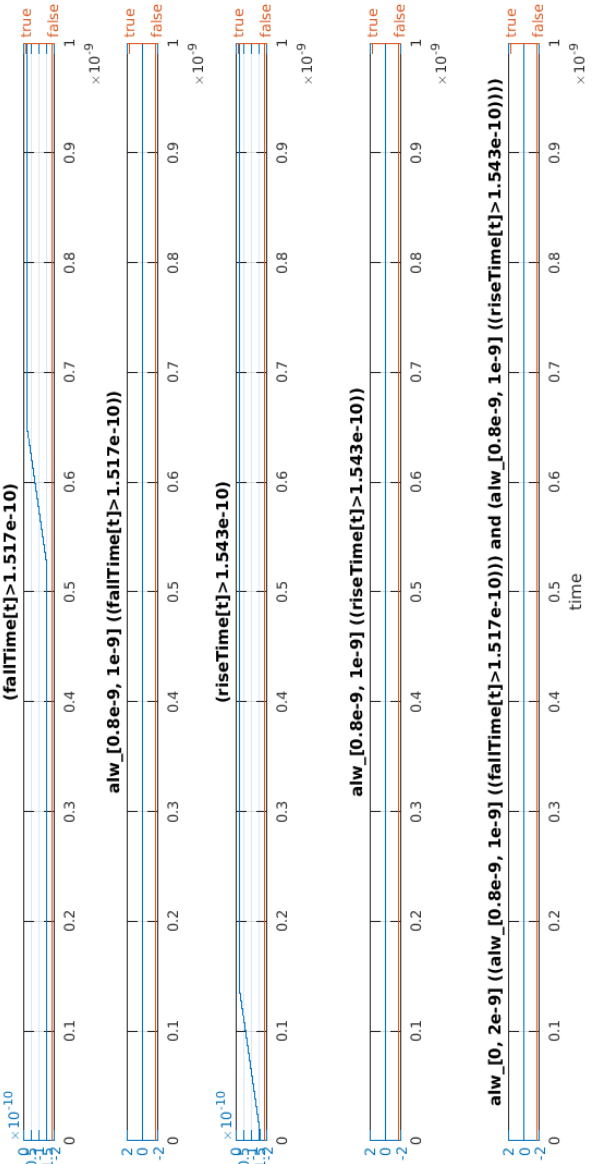
The terms riseTime[t] and fallTime[t] refer to the values of signal riseTime and fallTime at a time t, respectively. The function is a conjunction of monotonic objectives requiring each parameter to change monotonically. With respect to Figure 6.1 in Chapter 6, it may be noted that at 0.8 ns the output of the inverter has risen and stabilised and stays that way until the falling edge of the input signal. Thus in the time interval 0.8-1 ns, it is checked whether phi_ok is satisfied (i.e. risetime>min_tr and falltime>min_tf).

A two dimensional (2D) search algorithm has been presented to search the optimal nMOS transistor width and pMOS transistor width that satisfies the STL property. The optimal value of nMOS transistor width and pMOS transistor width have been derived from the range of the parameter obtained in Algorithm 1. The parameter range where nmax, nmin is the upper bound and lower bound of nMOS transistor width, respectively. Parameters pmax, pmin are the upper bound and lower bound of pMOS transistor width, resp. as shown in Algorithm 2. For STL property (risetime>min_tr and falltime>min_tf, where min_tr is 0.1543e-9 and min_tf is 0.1517e-9), the parameter range for nMOS transistor width is 2.4201 - 2.9041 and parameter range for pMOS transistor width is 3.4569 - 4.1482 (where nmin = 2.4201, nmax = 2.9041; pmin = 3.4569, pmax = 4.1482). Figure 5.6 depicts how the algorithm searches for an optimal nMOS and pMOS transistor width to satisfy the STL properties and the iteration is explained below.



(a) Lower bound that satisfies the STL property

Figure 5.4: pMOS and nMOS transistor width (μm) for STL property `riseTime[t] > min_tr` and `fallTime[t] > min_tf`.



(b) Upper bound that does not satisfies the STL property

Figure 5.4: pMOS and nMOS transistor width (μm) for STL property `riseTime[t] > min_tr` and `fallTime[t] > min_tf`.

Algorithm 1: Algorithm to identify search range for STL formula where objective function components vary monotonically with wn and wp

```
Data: delta=0.00001; wp0 = p0; wn0 = n0 m = m0
   /* m0=multiplying/dividing factor, other initialisations        */
model=BreachSimulinkSystem(modelname) /* create Breach model      */
result = cmosBreach(model, wp0, wn0) /* evaluates STL prop on
   model                                                           */
while true do
    prev=result;
    result = cmosBreach(model, wp0, wn0) /* evaluates STL prop on
       model                                                       */
    wn1 = wn0;
    wp1 = wp0;
    if result > 0 then
        /* satisfying trace found                                 */
        wn0 = wn0 × m; wp0 = wp0 × m;
        /* Now, the result was greater than 0, so it multiplies the
           transistor width with the multiplying factor such that the
           rise time and fall time decreases below min_tr and min_tf
           and returns first false value.                         */
    else
        wp0 = wp0 / m; wn0 = wn0 / m;
        /* If initially, the result was less than 0, it divides the
           transistor width with the dividing factor such that the
           monotonic objective fn increass above min_tr and min_tf and
           returns first true value.                              */
    end
    if (result != prev) then
        wNmin = min(wn0, wn1); wNmax = max(wn0, wn1);
        wPmin = min(wp0, wp1); wPmax = max(wp0, wp1);
        break;
        /* search range is identified                             */
    else
    end
end
[wN, wP] = search2d(model, wNmin, wNmax, wPmin, wPmax, delta)
```

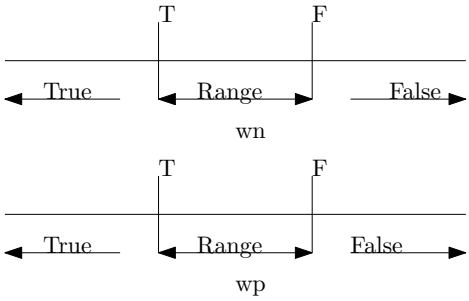


Figure 5.5: Data range using Algorithm 1.

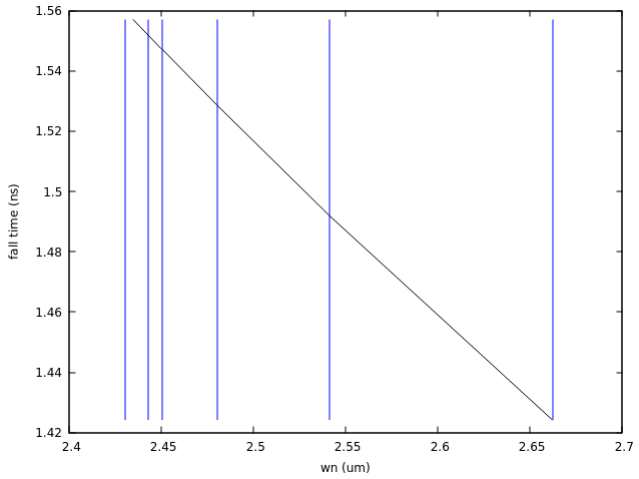
(a) From the parameter range of nMOS transistor width, we get the new-value of nMOS transistor width (the new-value, wn0=2.6621, i.e. mid-value of (nmin+nmax)/2). The STL property checks for the transistor width wn0, pmax. If the property does not satisfy, then we get new - value of pMOS transistor width (wp0= 3.8025, i.e. mid-value of (pmin+pmax)/2). We get new value from left side of the range.

(b) We get the new-value of nMOS transistor width (the new-value, wn1=2.5411, i.e. midvalue of (nmin+wn0)/2). STL property checks for the transistor width wn1, wp0. The property does not satisfy, then we get new - value of pMOS transistor width (wp1= 3.6247, i.e. midvalue of (wp0+pmin)/2). We get new value from left side of the range.

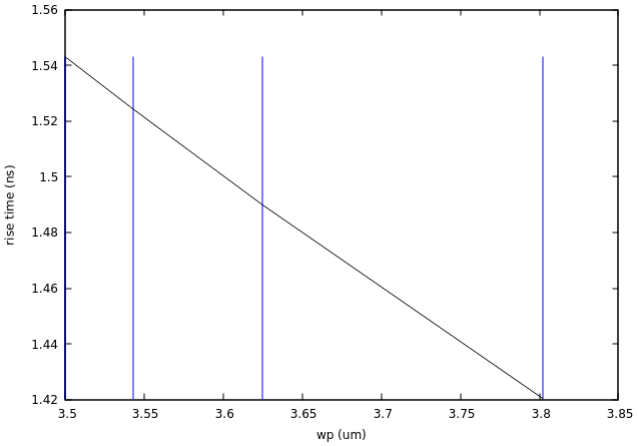
(c) We get the new-value of nMOS transistor width (the new-value, wn2=2.4807, i.e. midvalue of (nmin+wn1)/2). STL property checks for the transistor width wn2, wp1. The property does not satisfy, then we get new - value of pMOS transistor width (wp2= 3.5432, i.e. midvalue of (wp1+pmin)/2). We get new value from left side of the range.

(d) We get the new-value of nMOS transistor width (the new-value, wn3=2.4503, i.e. midvalue of (nmin+wn2)/2). STL property checks for the transistor width wn3, wp2. The property does not satisfy, then we get new - value of pMOS transistor width (wp3= 3.50007, i.e. midvalue of (wp2+pmin)/2). We get new value from left side of the range.

(e) We get the new-value of nMOS transistor width (the new-value, wn4=2.4351, i.e. midvalue of (nmin+wn3)/2). STL property checks for the transistor width wn4, wp3. The property does not satisfy, then we get new - value of pMOS transistor width (wp4=



(a)



(b)

Figure 5.6: 2D search for computation of rise time and fall time using Algorithm 2 for STL property `riseTime[t]` $>$ `min_tr` and `fallTime[t]` $>$ `min_tf`.

3.50007, i.e. midvalue of (wp3+pmin)/2). We get new value from left side of the range. Optimal value obtained is wn4, wp4.

Similarly, in the time interval 0.8–1 ns to check whether phi_ok is satisfied (ie risetime<max_tr and falltime<max_tf), the STL property is developed to capture the performance requirements at time t of CMOS inverter is described below.

```
param max_tr = 0.1570 e-9,
param max_tf = 0.1555 e-9
phitr_gr := riseTime[t] < max_tr
phitf_gr := fallTime[t] < max_tf
phi_ok := alw_[0.8e-9,1e-9] (phitr_gr and phitf_gr)
alw_phi := alw_[0, 1e-9](phi_ok)
```

For STL property (risetime<max_tr and falltime<max_tf, where max_tr is 0.1570e-9 and max_tf is 0.1555e-9), the parameter range for nMOS transistor width is 2.4201 - 2.9041 and parameter range for pMOS transistor width is 3.4569 - 4.1482 (where nmin = 2.4201, nmax = 2.9041; pmin = 3.4569, pmax = 4.1482). The lower bound consists of nMOS and pMOS transistor width that does not satisfies the STL property, shown in Figure 5.7a. The upper bound consists of nMOS and pMOS transistor width that satisfy the STL property, shown in Figure 5.7b.

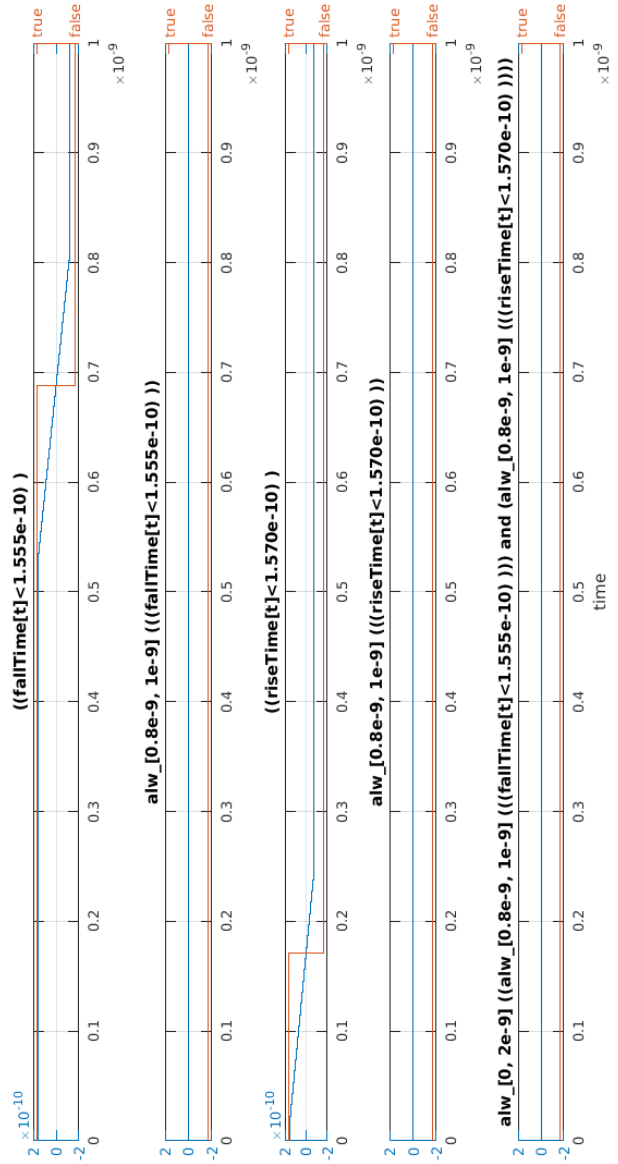
A two dimensional (2D) search algorithm has been presented to search the optimal nMOS transistor width and pMOS transistor width that satisfies the STL property. The optimal value of nMOS transistor width and pMOS transistor width has been derived from the range of the parameter obtained in Algorithm 1. Figure 5.8 depicts how the algorithm searches for an optimal nMOS and pMOS transistor width to satisfy the STL properties and the iteration is explained below.

(a) From the parameter range of nMOS transistor width, we get the new-value of nMOS transistor width (the new-value, wn0=2.6621, i.e. midvalue of (nmin+nmax)/2). STL property checks for the transistor width wn0, pmax. If the property does not satisfy, then we calculate a new - value of pMOS transistor width (wp0, i.e. midvalue of (pmin+pmax)/2). Here, for given pMOS transistor width (pmax = 4.1482), the STL property satisfy. So, we will further check for the optimal nMOS and pMOS transistor width.

(b) We get the new-value of nMOS transistor width (the new-value, wn1=2.5411, i.e. midvalue of (nmin+wn0)/2). STL property checks for the transistor width wn2, pmax. Here, for given pMOS transistor width (pmax = 4.1482), the STL property satisfy. So,

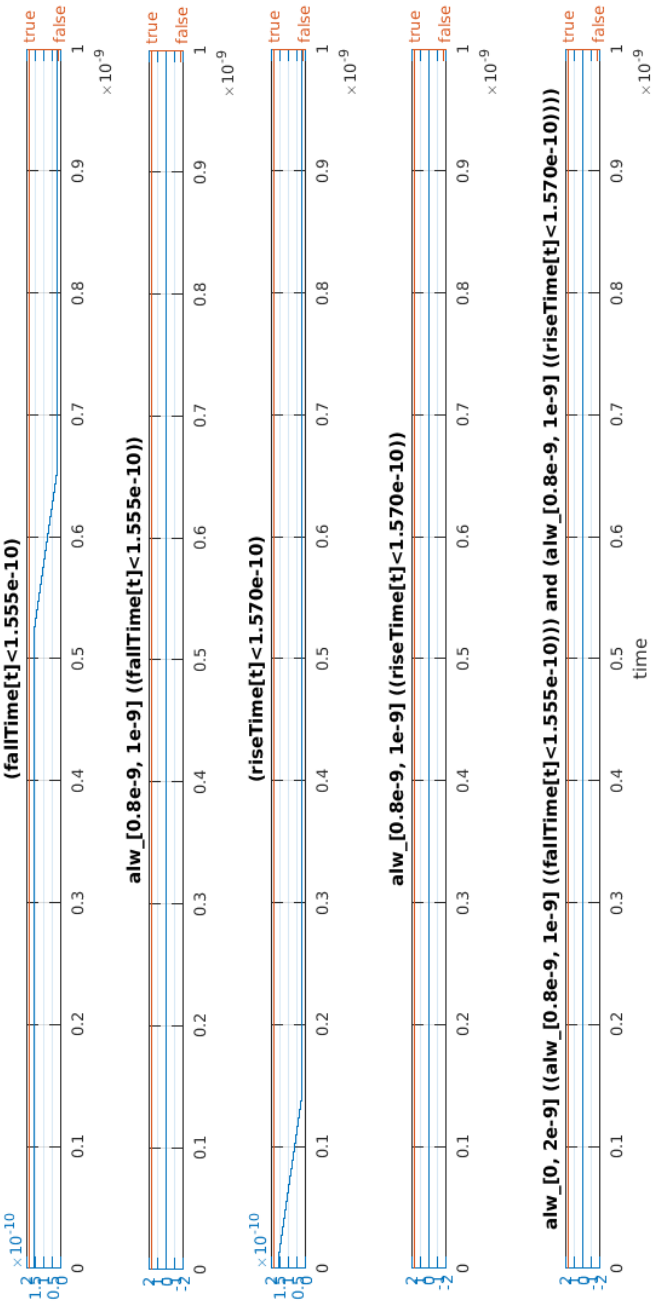
Algorithm 2: 2D search for parameter estimation

```
Input: wnmax=nmax /* nmax=UB of nMOS trans width */
wnmin=nmin /* nmin=LB of nMOS trans width */
wpmax=pmax /* pmax=UB of pMOS trans width */
wpmin =pmin/* pmin=LB of pMOS trans width */
Output: wn, wp
function [wn, wp] = search2d(model, wnmax, wnmin, wpmax,
  wpmin, delta)
c1 = cmosBreach(model, wpmin, wnmin)
c2 = cmosBreach(model, wpmax, wnmax)
/* evaluates STL prop on model */
wp=wpmin; /* lower bound of pMOS transistor width */
while true do
    wn = (wnmax+wnmin) / 2; /* mid-value of nMOS transistor width
       */
    y= cmosBreach(model, wp, wn); /* evaluates STL prop on model
       */
    if (y is false) then
        wp=(wpmax+wpmin) / 2 ; /* mid-value of pMOS transistor
           width */
    end
    if |wnmax − wnmin| and |wpmax − wpmin| < delta then
        break;
    end
    if c1 == y then
        wnmin = wn; wpmin = wp;
        /* transistor width is identified in the right half */
    else
        wnmax = wn; wpmax = wp;
        /* transistor width is identified in the left half */
    end
end
```



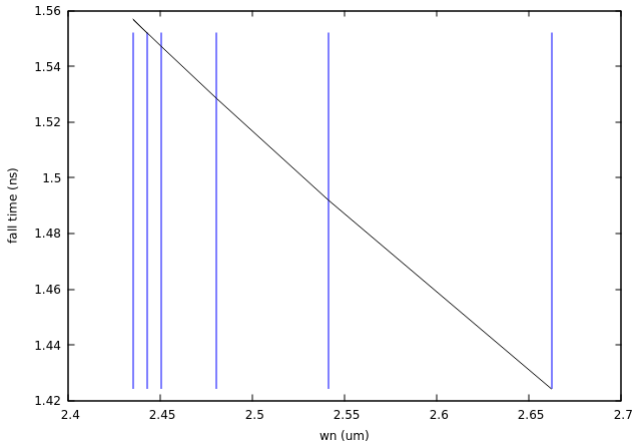
(a) Lower bound that does not satisfies the STL property

Figure 5.7: pMOS and nMOS transistor width (μm) for STL property `riseTime[t]` $<$ `max_tr` and `fallTime[t]` $<$ `max_tf`.

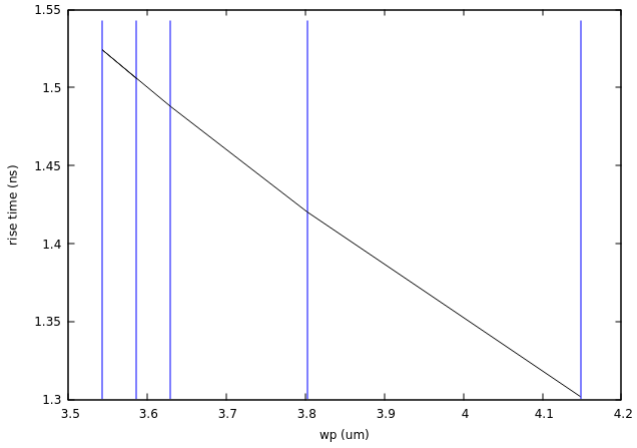


(b) Upper bound that satisfies the STL property

Figure 5.7: pMOS and nMOS transistor width (μm) for STL property `riseTime[t]` $<$ `max_tr` and `fallTime[t]` $<$ `max_tf`.



(a)



(b)

Figure 5.8: 2D search for computation of rise time and fall time using Algorithm 2 for STL property `riseTime[t]` $<$ `max_tr` and `fallTime[t]` $<$ `max_tf`.

we will further check for the optimal nMOS and pMOS transistor width.

(c) We get the new-value of nMOS transistor width (the new-value, wn2=2.4807, i.e. midvalue of (nmin+wn1)/2). STL property checks for the transistor width wn2, pmax. The property does not satisfy, then we get new - value of pMOS transistor width (wp0 = 3.8026, i.e. midvalue of (pmax+pmin)/2)). We get new value from left side of the range.

(d) We get the new-value of nMOS transistor width (the new-value, wn3=2.4503, i.e. midvalue of (nmin+wn2)/2). STL property checks for the transistor width wn3, wp0. The property does not satisfy, then we get new - value of pMOS transistor width (wp1 = 3.6297, i.e. midvalue of (pmin +wp0)/2). We get new value from left side of the range.

(e) We get the new-value of nMOS transistor width (the new-value, wn4=2.4352, i.e. midvalue of (nmin+wn3)/2). STL property checks for the transistor width wn4, wp1. The property does not satisfy, then we get new - value of pMOS transistor width (wp2= 3.5433, i.e. midvalue of (pmin+wp1)/2). We get new value from left side of the range.

(f) We get the new-value of nMOS transistor width (the new-value, wn5=2.4427, i.e. midvalue of (wn3+nmin)/2), new nmin is equal to wn4. STL property checks for the transistor width wn5, wp1. The property does not satisfy, then we get new - value of pMOS transistor width (wp3= 3.5865, i.e. midvalue of (pmin+wp1)/2), where new pmin is wp2. We get new value from left side of the range. Optimal value obtained is wn5, wp3.

It is important to note that the function defined below does not work because for the riseTime to be greater than min_tr, the pMOS transistor width must increase, whereas for the riseTime to be less than max_tr, the pMOS transistor width must increase.

```
param min_tr = 0.1543 e-9,
param max_tr = 0.1570 e-9
phitr_lw := riseTime[t] > min_tr
phitr_lw := riseTime[t] < max_tr
phi_ok := alw_[0.8e-9,1e-9] (phitr_lw and phitr_gr)
alw_phi := alw_[0, 1e-9](phi_ok)
```

b) **Computation of power dissipation**

The power dissipation is computed by applying a steep ramp as input to the CMOS inverter. The rise and fall times of the ramp should be chosen less than the output rise time and fall time in order to achieve minimum dissipation [46].

The peak power dissipation or the average power may be considered. Power dissipated at pMOS and nMOS transistor are indicated in (5.3) and (5.4) respectively.

$$P_{\mathrm{p}} = I_{\mathrm{p}} \cdot (V_{\mathrm{dd}} - V_{\mathrm{out}}) \tag{5.3}$$

P_{p} is captured in regions A and A2.

$$P_{\mathrm{n}} = I_{\mathrm{n}} \cdot V_{\mathrm{out}} \tag{5.4}$$

P_{n} is captured in regions E and E1.
The short circuit power dissipation is calculated using equation (5.5)

$$P_{\mathrm{sc}} = \frac{V_{\mathrm{dd}}}{\mathrm{T}} \int_0^{\mathrm{T}} i_{\mathrm{sc}}(t)dt \tag{5.5}$$

The short circuit power dissipation is determined by the power dissipated in regions B and C.

$$\text{power dissipation} \propto (\mathrm{w_p}, \mathrm{w_n}) \tag{5.6}$$

As done earlier, for computing power dissipation also, a range of values is obtained from the given initial value of pMOS transistor width and nMOS transistor width, where p0 = 2.0 μm and n0 = 1.4 μm respectively. The lower bound consists of nMOS and pMOS transistor width that satisfies the STL property, shown in Figure 5.10a. The upper bound consists of nMOS and pMOS transistor width that does not satisfy the STL property, shown in Figure 5.10b. From equation (5.6), power dissipation is directly proportional to the nMOS transistor width and pMOS transistor width. With increase in nMOS transistor width and pMOS transistor width, power dissipation will increase, as depicted in Figure 5.9. So if the power disipation increases above max_psc (max_psc is the maximum power dissipation that can be achieved), we get the upper bound value i.e. the first *false* value that does not satisfy the STL property, beyond which all values are *false*. For power disipation below max_psc, we get the lower bound value i.e. the *true* value that satisfies the STL property, beyond which all values are *true*.

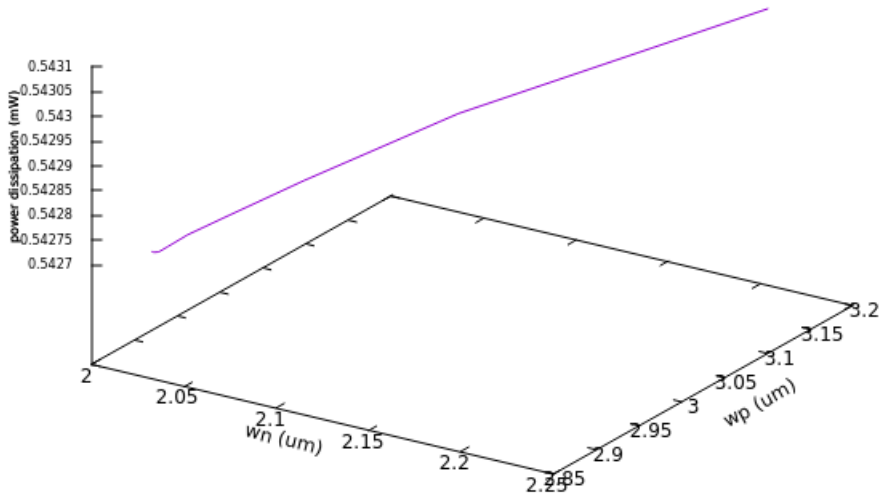


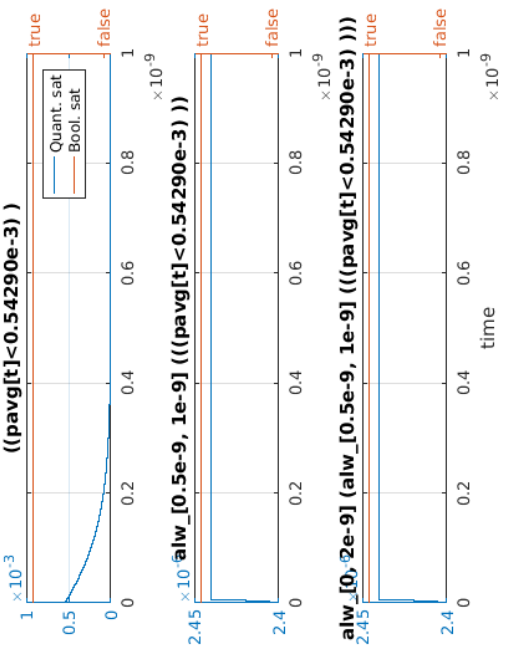
Figure 5.9: Transistor width (μm) vs power dissipation (mW) of CMOS inverter.

The STL property developed to capture the performance requirements at time t of CMOS inverter for `psc[t]` $<$ `max_psc` (max_psc is the maximum power that can be achieved) using 2D search algorithm to minimize power dissipation is described below.

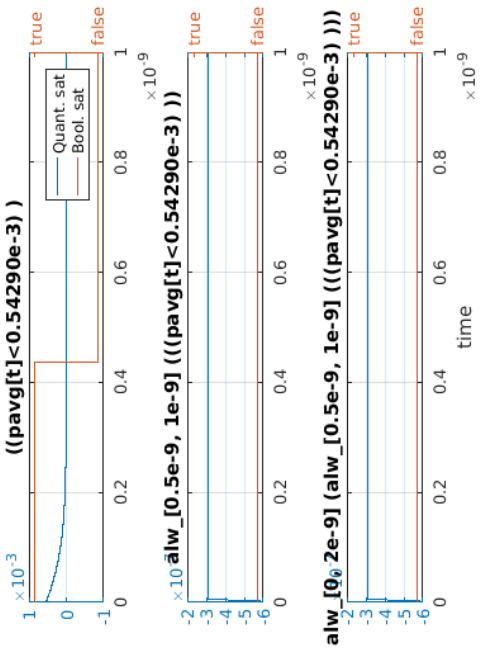
```
param max_psc = 0.54290 e-3
phitr_gr := psc[t] < max_psc
phipsc_ok := alw_[0.22e-9, 1e-9](phi_psc)
alw_phi := alw_[0, 1e-9](phipsc_ok)
```

The term psc[t] refers to the value of signal power dissipation at a time t. For STL property (`psc[t]` $<$ `max_psc`, where max_psc is 0.54290e-3), the parameter range for nMOS transistor width is 2.0167 - 2.4201 and parameter range for pMOS transistor width is 2.8807 - 3.4569 (where nmin = 2.0167, nmax = 2.4201; pmin = 2.8807, pmax =3.4569).

A two dimensional (2D) search algorithm has been presented to search the optimal nMOS transistor width and pMOS transistor width that satisfies the STL property. The optimal value of nMOS transistor width



(a) Lower bound that satisfies the STL property



(b) Upper bound that does not satisfies the STL property

Figure 5.10: pMOS and nMOS transistor width (μm)for STL property `psc[t] < max_psc`.

and pMOS transistor width has been derived from the range of the parameter obtained in Algorithm 1. Figure 5.11 depicts how the algorithm searches for an optimal nMOS and pMOS transistor width to satisfy the STL properties and the iteration is explained below.

(a) From the parameter range of nMOS transistor width, we get the new-value of nMOS transistor width (the new-value, wn0=2.2184, i.e. midvalue of (nmin+nmax)/2). STL property checks for the transistor width wn0, pmax. If the property does not satisfy, then we get new - value of pMOS transistor width (wp0= 3.1688, i.e. midvalue of (pmin+pmax)/2). We get new value from left side of the range.

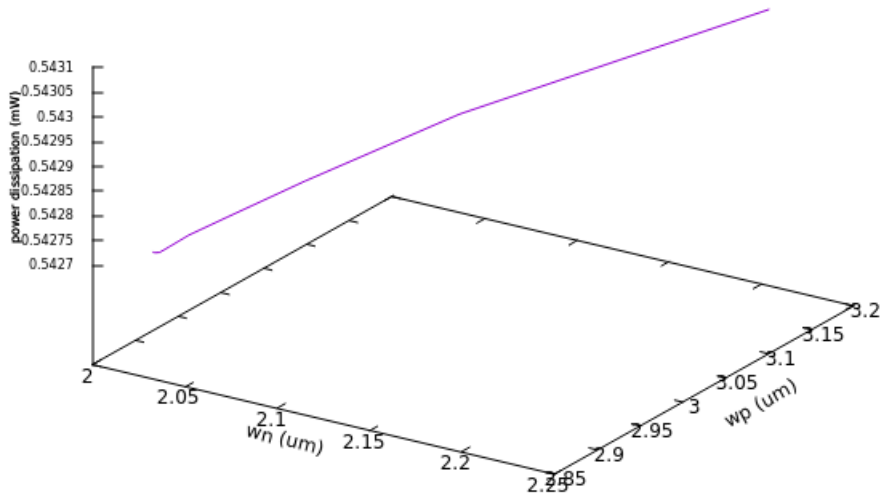
(b) We get the new-value of nMOS transistor width (the new-value, wn1=2.1176, i.e. midvalue of (nmin+wn0)/2). STL property checks for the transistor width wn1, wp0. The property does not satisfy, then we get new - value of pMOS transistor width (wp1= 3.0248, i.e. midvalue of (wp0+pmin)/2). We get new value from left side of the range.

(c) We get the new-value of nMOS transistor width (the new-value, wn2=2.0671, i.e. midvalue of (nmin+wn1)/2). STL property checks for the transistor width wn2, wp1. The property does not satisfy, then we get new - value of pMOS transistor width (wp2= 2.9527, i.e. midvalue of (wp1+pmin)/2). We get new value from left side of the range.

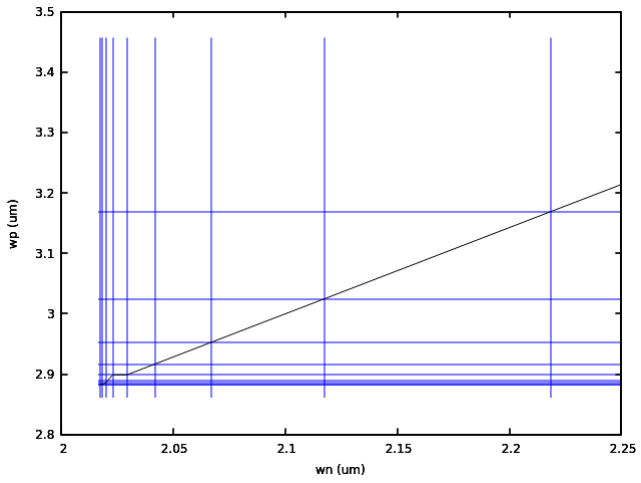
(d) We get the new-value of nMOS transistor width (the new-value, wn3=2.0419, i.e. midvalue of (nmin+wn2)/2). STL property checks for the transistor width wn3, wp2. The property does not satisfy, then we get new - value of pMOS transistor width (wp3= 2.9167, i.e. midvalue of (wp2+pmin)/2). We get new value from left side of the range.

(e) We get the new-value of nMOS transistor width (the new-value, wn4=2.02931, i.e. midvalue of (nmin+wn3)/2). STL property checks for the transistor width wn4, wp3. The property does not satisfy, then we get new - value of pMOS transistor width (wp4= 2.8987, i.e. midvalue of (wp3+pmin)/2). We get new value from left side of the range.

(f) We get the new-value of nMOS transistor width (the new-value, wn5=2.0230, i.e. midvalue of (nmin+wn4)/2). STL property checks for the transistor width wn5, wp4. The property does not satisfy, then we get new - value of pMOS transistor width (wp5=



(a)



(b)

Figure 5.11: 2D search for computation of power dissipation using Algorithm 2 for STL property `psc[t]` $<$ `max_psc`.

2.8897, i.e. midvalue of (wp4+pmin)/2). We get new value from left side of the range.

(g) We get the new-value of nMOS transistor width (the new-value, wn6=2.0199, i.e. midvalue of (nmin+wn5)/2). STL property checks for the transistor width wn6, wp5. The property does not satisfy, then we get new - value of pMOS transistor width (wp6= 2.8852, i.e. midvalue of (wp5+pmin)/2). We get new value from left side of the range.

(h) We get the new-value of nMOS transistor width (the new-value, wn7=2.0183, i.e. midvalue of (nmin+wn6)/2). STL property checks for the transistor width wn7, wp6. The property does not satisfy, then we get new - value of pMOS transistor width (wp7= 2.8830, i.e. midvalue of (wp6+pmin)/2). We get new value from left side of the range.

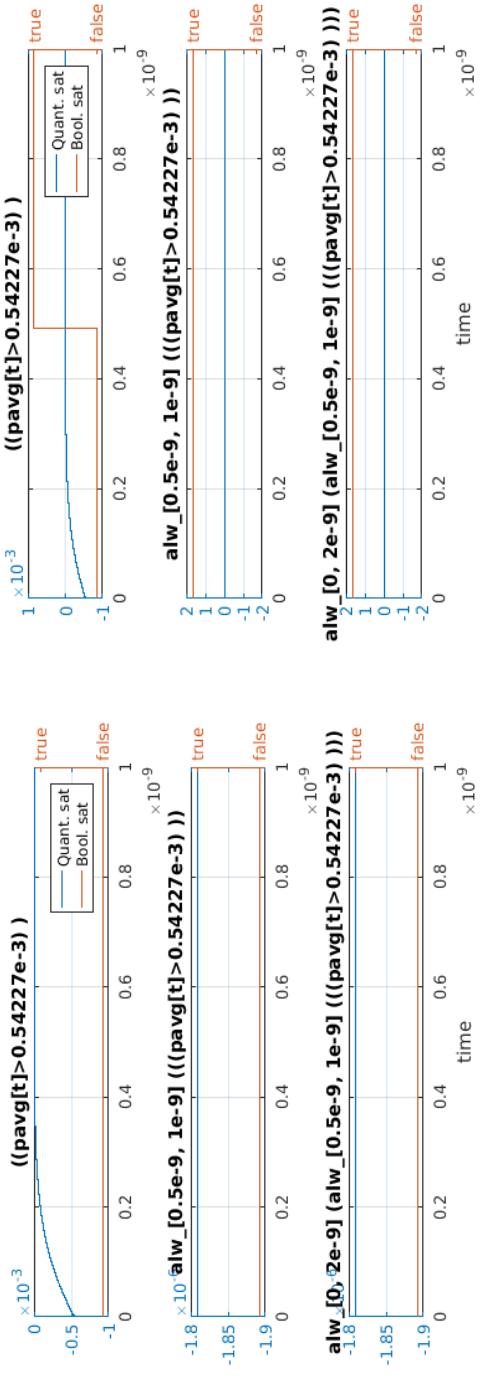
(i) We get the new-value of nMOS transistor width (the new-value, wn8=2.0175, i.e. midvalue of (nmin+wn7)/2). STL property checks for the transistor width wn8, wp7. The property does not satisfy, then we get new - value of pMOS transistor width (wp8= 2.8829, i.e. midvalue of (wp7+pmin)/2). We get new value from left side of the range. Optimal value obtained is wn8, wp8.

Similary, STL property for `psc[t] > min_psc` (min_psc is the minimum power that can be achieved) to capture the performance requirements at time t of CMOS inverter is described below.

```
param min_psc = 0.54227 e-3
phitr_gr := psc[t] > min_psc
phipsc_ok := alw_[0.22e-9, 1e-9](phi_psc)
alw_phi := alw_[0, 1e-9](phipsc_ok)
```

For STL property (`psc[t] > min_psc`, where min_psc is 0.54227e-3), the parameter range for nMOS transistor width is 1.9005 - 2.2806 and parameter range for pMOS transistor width is 2.7005 - 3.2406 (where nmin = 1.9005, nmax = 2.2806; pmin = 2.7005, pmax =3.2406). The lower bound consists of nMOS and pMOS transistor width that does not satisfies the STL property, shown in Figure 5.12a. The upper bound consists of nMOS and pMOS transistor width that satisfy the STL property, shown in Figure 5.12b.

A two dimensional (2D) search algorithm has been presented to search the optimal nMOS transistor width and pMOS transistor width that satisfies the STL property. The optimal value of nMOS transistor width



(a) Lower bound that does not satisfies the STL property

(b) Upper bound that satisfies the STL property

Figure 5.12: pMOS and nMOS transistor width (μm) for STL property `psc[t] > min_psc`.

and pMOS transistor width has been derived from the range of the parameter obtained in Algorithm 1. Figure 5.13 depicts how the algorithm searches for an optimal nMOS and pMOS transistor width to satisfy the STL properties and the iteration is explained below.

(a) From the parameter range of nMOS transistor width, we get the new-value of nMOS transistor width (the new-value, wn0=2.0906, i.e. midvalue of (nmin+nmax)/2). STL property checks for the transistor width wn0, pmax. If the property does not satisfy, then we get new - value of pMOS transistor width (wp0= 2.9705, i.e. midvalue of (pmin+pmax)/2). We get new value from left side of the range.

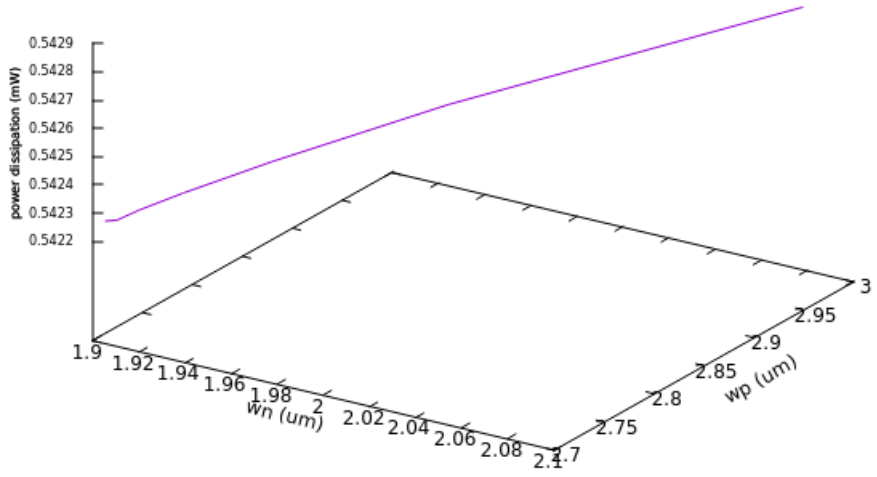
(b) We get the new-value of nMOS transistor width (the new-value, wn1=1.9955, i.e. midvalue of (nmin+wn0)/2). STL property checks for the transistor width wn1, wp0. The property does not satisfy, then we get new - value of pMOS transistor width (wp1= 2.8355, i.e. midvalue of (wp0+pmin)/2). We get new value from left side of the range.

(c) We get the new-value of nMOS transistor width (the new-value, wn2=1.9480, i.e. midvalue of (nmin+wn1)/2). STL property checks for the transistor width wn2, wp1. The property does not satisfy, then we get new - value of pMOS transistor width (wp2= 2.7680, i.e. midvalue of (wp1+pmin)/2). We get new value from left side of the range.

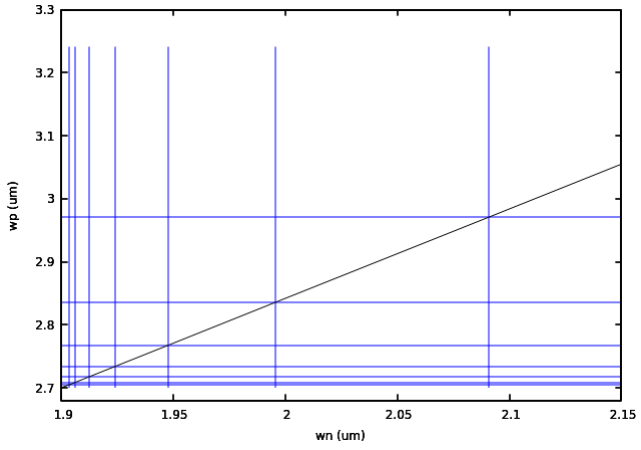
(d) We get the new-value of nMOS transistor width (the new-value, wn3=1.9243, i.e. midvalue of (nmin+wn2)/2). STL property checks for the transistor width wn3, wp2. The property does not satisfy, then we get new - value of pMOS transistor width (wp3= 2.7343, i.e. midvalue of (wp2+pmin)/2). We get new value from left side of the range.

(e) We get the new-value of nMOS transistor width (the new-value, wn4=1.9124, i.e. midvalue of (nmin+wn3)/2). STL property checks for the transistor width wn4, wp3. The property does not satisfy, then we get new - value of pMOS transistor width (wp4= 2.7174, i.e. midvalue of (wp3+pmin)/2). We get new value from left side of the range.

(f) We get the new-value of nMOS transistor width (the new-value, wn5=1.9064, i.e. midvalue of (nmin+wn4)/2). STL property checks for the transistor width wn5, wp4. The property does not satisfy, then we get new - value of pMOS transistor width (wp5=



(a)



(b)

Figure 5.13: 2D search for computation of power dissipation using Algorithm 2 for STL property `psc[t] > min_psc`.

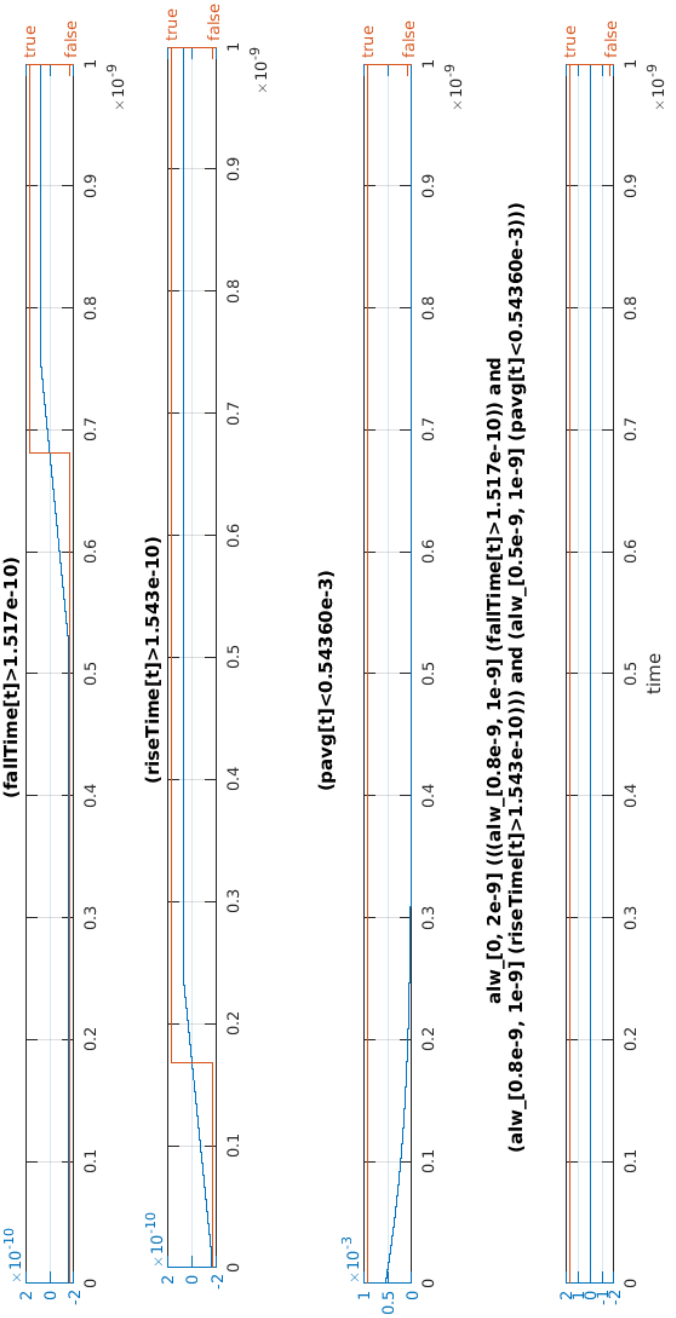
2.7089, i.e. midvalue of (wp4+pmin)/2). We get new value from left side of the range.

(g) We get the new-value of nMOS transistor width (the new-value, wn6=1.9035, i.e. midvalue of (nmin+wn5)/2). STL property checks for the transistor width wn6, wp5. The property does not satisfy, then we get new - value of pMOS transistor width (wp6= 2.7047, i.e. midvalue of (wp5+pmin)/2). We get new value from left side of the range. Optimal value obtained is wn6, wp6.

c) **Computation of rise time and fall time and power dissipation**

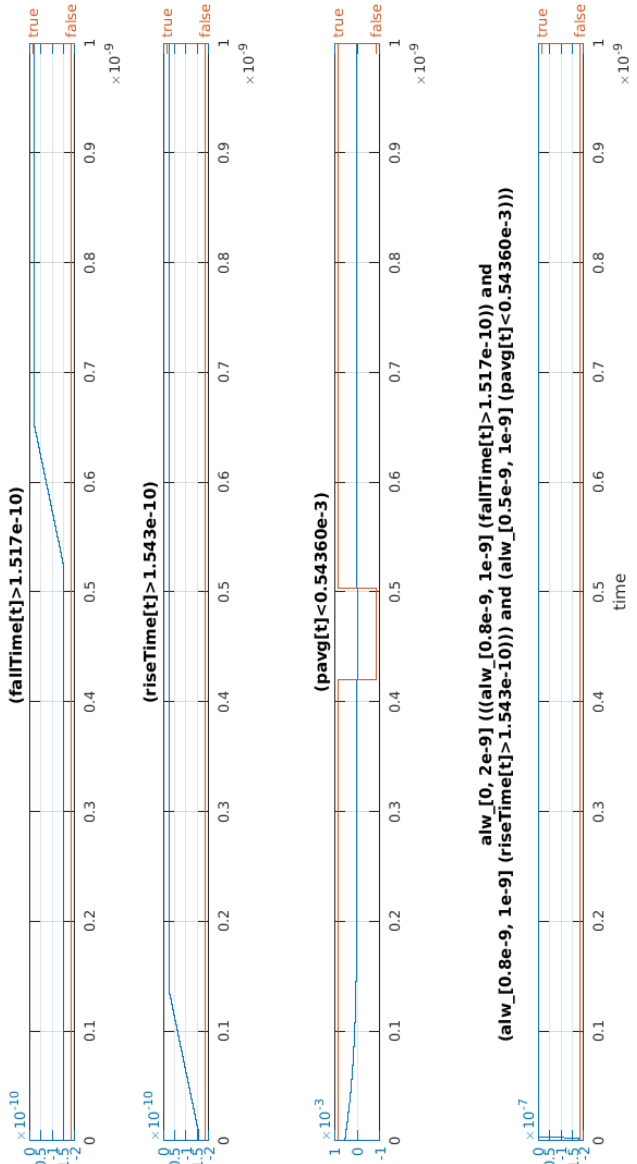
As done earlier, for computing rise time and fall time and power dissipation, a range of values is obtained from the given initial value of pMOS transistor width and nMOS transistor width, where p0 = 2.0 μm and n0 = 1.4 μm respectively. The lower bound consists of nMOS and pMOS transistor widths that satisfy the STL property. The upper bound represents nMOS and pMOS transistor widths that do not satisfy the STL property. As explained earlier, power dissipation is directly proportional to the nMOS transistor width and pMOS transistor width. The fall time is inversely proportional to the nMOS transistor width for a given pMOS transistor width. Similarly, rise time is inversely proportional to the pMOS transistor width, for a given nMOS transistor width. So if the power dissipation increase above max_psc (max_psc is the maximum power dissipation that can be achieved) and the rise time and fall time decrease below min_tr and min_tf, respectively, we get the upper bound value i.e., the first *false* value that does not satisfy the STL property, beyond which all values are *false*. For power dissipation below max_psc and rise time and fall time above min_tr and min_tf respectively, we get the lower bound value i.e., the *true* value that satisfies the STL property, beyond which all values are *true*. The lower bound consists of nMOS and pMOS transistor width that satisfies the STL property, shown in Figure 5.14a. The upper bound consists of nMOS and pMOS transistor width that does not satisfy the STL property, shown in Figure 5.14b. The STL property to find the performance requirements at time t of CMOS inverter using 2D search algorithm are described below.

```
param min_tr = 0.1543 e-9,
param min_tf = 0.1517 e-9,
param max_psc = 0.54360 e-3
phitr_lw := riseTime[t] > min_tr
phitf_lw := fallTime[t] > min_tf
```



(a) Lower bound that satisfies the STL property

Figure 5.14: pMOS and nMOS transistor width (μm) for STL property `riseTime[t] > min_tr` and `fallTime[t] > min_tf` and `psc[t] < max_psc`.



(b) Upper bound that does not satisfies the STL property

Figure 5.14: pMOS and nMOS transistor width (μm) for STL property `riseTime[t] > min_tr` and `fallTime[t] > min_tf` and `psc[t] < max_psc`.

```
phi_ok := alw_[0.8e-9,1e-9] (phitr_lw and phitf_lw)
phipsc_gr := psc[t] < max_psc
phipsc_ok := alw_[0.22e-9, 1e-9](phipsc_gr)
alw_phi := alw_[0, 1e-9](phi_ok and phipsc_ok )
```

The rise time and fall time and power is the objective function. For STL property (risetime>min_tr and falltime>min_tf and power `psc[t] < max_psc`, where min_tr is 0.1543e-9 and min_tf is 0.1517e-9, max_psc is 0.54360e-3), the parameter range for nMOS transistor width is 2.4201 - 2.9041 and parameter range for pMOS transistor width is 3.4569 - 4.1482 (where nmin = 2.4201, nmax = 2.9041; pmin = 3.4569 , pmax = 4.1482).

A two dimensional (2D) search algorithm has been presented to search the optimal nMOS transistor width and pMOS transistor width that satisfies the STL property. The optimal value of nMOS transistor width and pMOS transistor width has been derived from the range of the parameter obtained in Algorithm 1. Figure 5.15 depicts how the al-

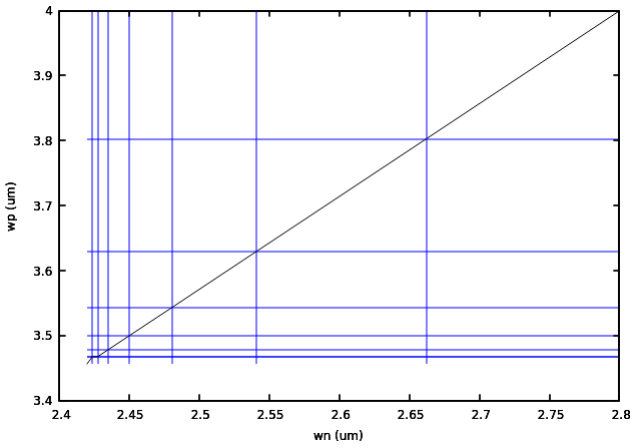


Figure 5.15: 2D search for computation of rise time and fall time and power dissipation using Algorithm 2 for STL property `riseTime[t] > min_tr` and `fallTime[t] > min_tf` and `psc[t] < max_psc`.

gorithm searches for an optimal nMOS transistor width to satisfy the STL properties and the iteration is explained below.

(a) From the parameter range of nMOS transistor width, we get the new-value of nMOS transistor width (the new-value, wn0=2.6621, i.e. midvalue of (nmin+nmax)/2). STL property checks for the transistor width wn0, pmax. If the property does not satisfy, then we get new - value of pMOS transistor width (wp0= 3.8026, i.e.

midvalue of (pmin+pmax)/2). We get new value from left side of the range.

(b) We get the new-value of nMOS transistor width (the new-value, wn1=2.5411, i.e. midvalue of (nmin+wn0)/2). STL property checks for the transistor width wn1, wp0. The property does not satisfy, then we get new - value of pMOS transistor width (wp1= 3.6297, i.e. midvalue of (wp0+pmin)/2). We get new value from left side of the range.

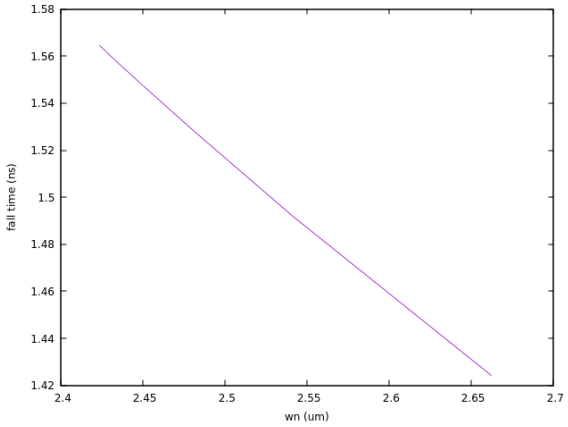
(c) We get the new-value of nMOS transistor width (the new-value, wn2=2.4806, i.e. midvalue of (nmin+wn1)/2). STL property checks for the transistor width wn2, wp1. The property does not satisfy, then we get new - value of pMOS transistor width (wp2= 3.5433, i.e. midvalue of (wp1+pmin)/2). We get new value from left side of the range.

(d) We get the new-value of nMOS transistor width (the new-value, wn3=2.4503, i.e. midvalue of (nmin+wn2)/2). STL property checks for the transistor width wn3, wp2. The property does not satisfy, then we get new - value of pMOS transistor width (wp3= 3.5001, i.e. midvalue of (wp2+pmin)/2). We get new value from left side of the range.

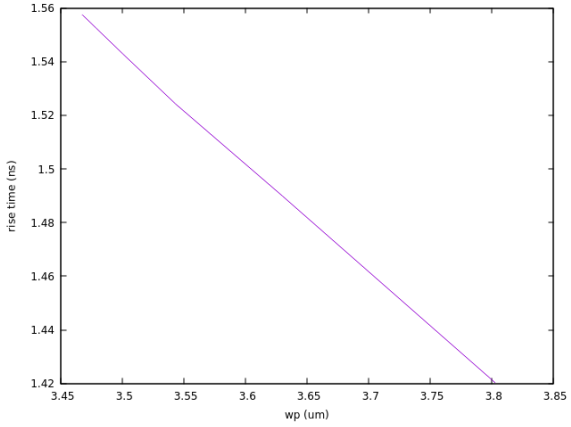
(e) We get the new-value of nMOS transistor width (the new-value, wn4=2.4312, i.e. midvalue of (nmin+wn3)/2). STL property checks for the transistor width wn4, wp3. The property does not satisfy, then we get new - value of pMOS transistor width (wp4= 3.4785, i.e. midvalue of (wp3+pmin)/2). We get new value from left side of the range.

(f) We get the new-value of nMOS transistor width (the new-value, wn5=2.4276, i.e. midvalue of (nmin+wn4)/2). STL property checks for the transistor width wn5, wp4. The property does not satisfy, then we get new - value of pMOS transistor width (wp5= 3.4677, i.e. midvalue of (wp4+pmin)/2). We get new value from left side of the range.

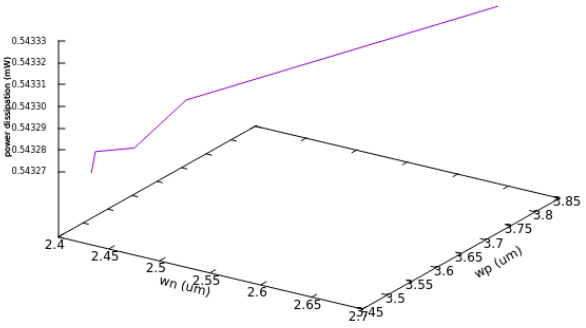
(g) We get the new-value of nMOS transistor width (the new-value, wn6=2.4238, i.e. midvalue of (nmin+wn5)/2). STL property checks for the transistor width wn6, wp5. The property does not satisfy, then we get new - value of pMOS transistor width (wp6= 3.4676, i.e. midvalue of (wp5+pmin)/2). We get new value from left side of the range. Optimal value obtained is wn6, wp6.



(a)



(b)



(c)

Figure 5.16: Objective function with respect to transistor width (w_{n} and w_{p}).

Similary, the STL property developed where, `riseTime[t]` $<$ `max_tr` and `fallTime[t]` $<$ `max_tf` and `psc[t]` $>$ `min_psc` to capture the performance requirements at time t of CMOS inverter.

```
param max_tr = 0.1570 e-9,
param max_tf = 0.1555 e-9,
param min_psc = 0.54320 e-3
phitr_lw := riseTime[t] < max_tr
phitf_lw := fallTime[t] < max_tf
phi_ok := alw_[0.8e-9,1e-9] (phitr_lw and phitf_lw)
phipsc_gr := psc[t] > min_psc
phipsc_ok := alw_[0.22e-9, 1e-9](phipsc_gr)
alw_phi := alw_[0, 1e-9](phi_ok and phipsc_ok )
```

For STL property (risetime<max_tr and falltime<max_tf and power `psc[t]` $>$ `min_psc`, where max_tr is 0.1570e-9 and max_tf is 0.1555e-9, min_psc is 0.54320e-3), the parameter range for nMOS transistor width is 2.4201 - 2.9041 and parameter range for pMOS transistor width is 3.4569 - 4.1482 (where nmin = 2.4201, nmax = 2.9041; pmin = 3.4569 , pmax = 4.1482). The lower bound consists of nMOS and pMOS transistor width that does not satisfies the STL property, shown in Figure 5.17a. The upper bound consists of nMOS and pMOS transistor width that satisfy the STL property, shown in Figure 5.17b.

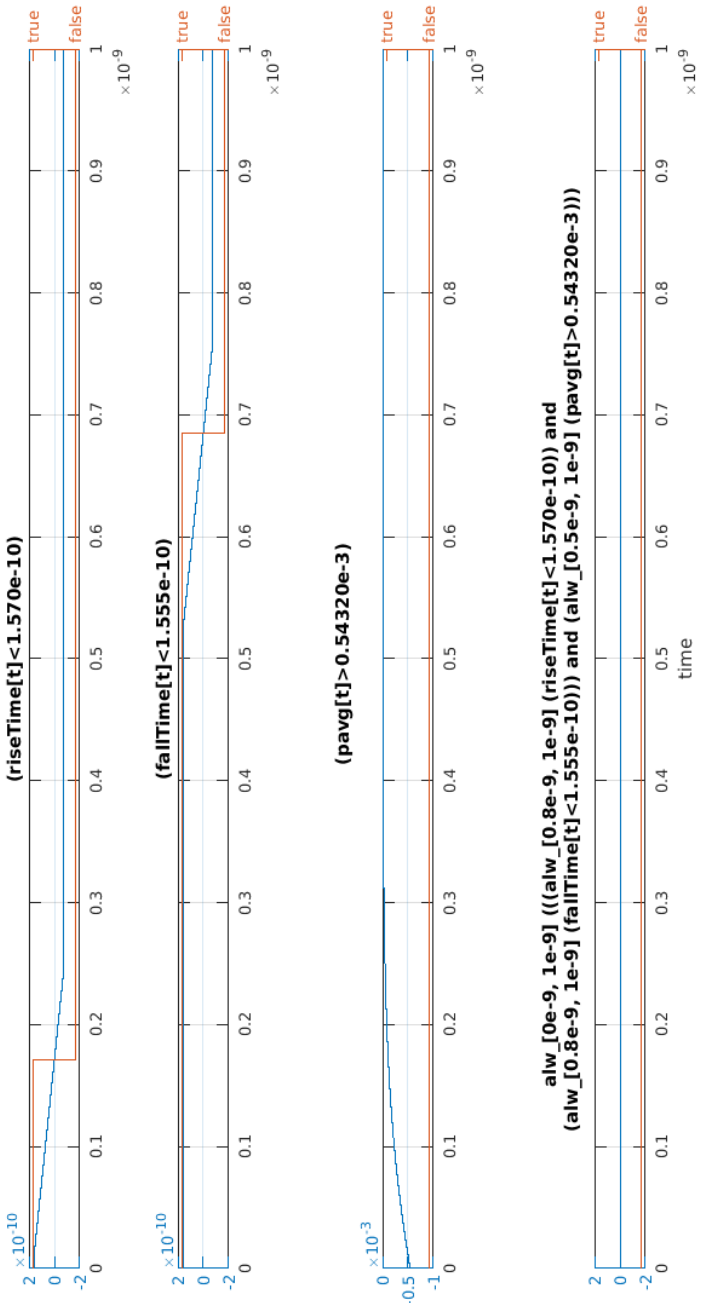
A two dimensional (2D) search algorithm has been presented to search the optimal nMOS transistor width and pMOS transistor width that satisfies the STL property. The optimal value of nMOS transistor width and pMOS transistor width has been derived from the range of the parameter obtained in Algorithm 1. Figure 5.18 depicts how the algorithm searches for an optimal nMOS transistor width to satisfy the STL properties and the iteration is explained below.

(a) From the parameter range of nMOS transistor width, we get the new-value of nMOS transistor width (the new-value, wn0=2.6621, i.e. midvalue of (nmin+nmax)/2). STL property checks for the transistor width wn0, pmax. If the property does not satisfy, then we get new - value of pMOS transistor width (wp0= 3.8026, i.e. midvalue of (pmin+pmax)/2). We get new value from left side of the range.

(b) We get the new-value of nMOS transistor width (the new-value, wn1=2.5411, i.e. midvalue of (nmin+wn0)/2). STL property checks for the transistor width wn1, wp0. The property does not satisfy, then we get new - value of pMOS transistor width (wp1=

(a) Lower bound that does not satisfies the STL property

Figure 5.17: pMOS and nMOS transistor width (μm) for STL property `risetime` < `max_tr` and `falltime` < `max_tf` and `psc[t]` > `min_psc`.



(b) Upper bound that satisfies the STL property

Figure 5.17: pMOS and nMOS transistor width (μm) for STL property `risetime` $<$ `max_tr` and `falltime` $<$ `max_tf` and `psc[t]` $>$ `min_psc`.

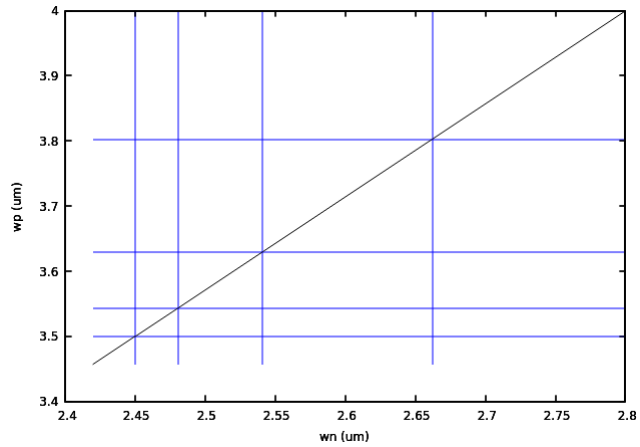


Figure 5.18: 2D search for computation of rise time and fall time and power dissipation using Algorithm 2 for STL property `risetime` < `max_tr` and `falltime` < `max_tf` and `psc[t]` > `min_psc`.

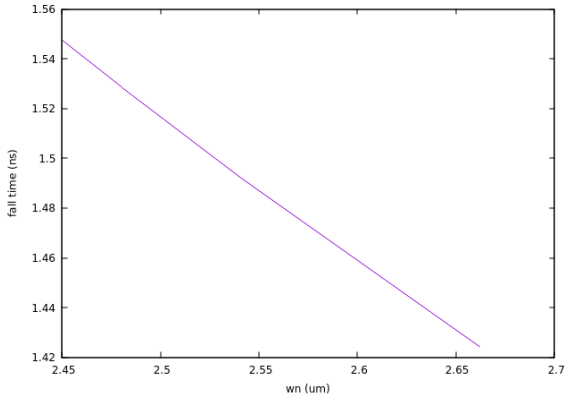
3.6297, i.e. midvalue of (wp0+pmin)/2). We get new value from left side of the range.

(c) We get the new-value of nMOS transistor width (the new-value, wn2=2.4806, i.e. midvalue of (nmin+wn1)/2). STL property checks for the transistor width wn2, wp1. The property does not satisfy, then we get new - value of pMOS transistor width (wp2= 3.5433, i.e. midvalue of (wp1+pmin)/2). We get new value from left side of the range.

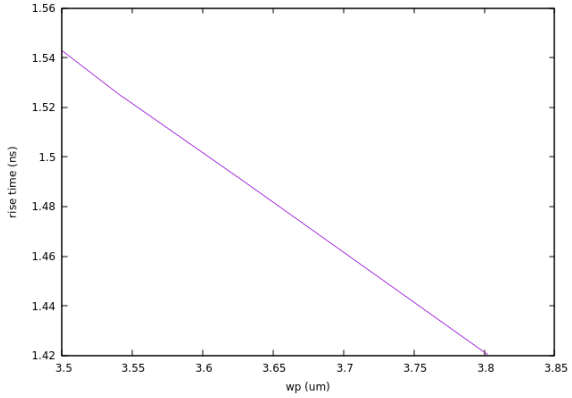
(d) We get the new-value of nMOS transistor width (the new-value, wn3=2.4503, i.e. midvalue of (nmin+wn2)/2). STL property checks for the transistor width wn3, wp2. The property does not satisfy, then we get new - value of pMOS transistor width (wp3= 3.5001, i.e. midvalue of (wp2+pmin)/2). We get new value from left side of the range. Optimal value obtained is wn6, wp6.

5.2.2 Nelder Mead Algorithm

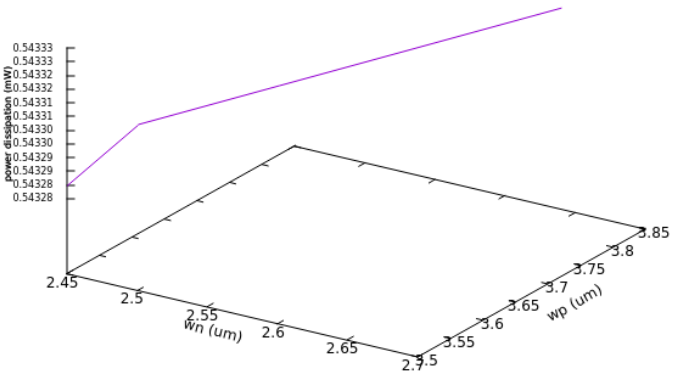
Breach tool of Matlab provides the function `max_sat_problem = MaxSatProblem(BrSys, phi, params, ranges)`, which attempts to find a set of parameters using the Nelder-Mead (NM) algorithms [81] [82] in the given ranges so that the given model with the identified parameters satisfies the STL formula, if possible, returning a positive value. Otherwise, in case of failure, a negative value is returned.



(a)



(b)



(c)

Figure 5.19: Objective function with respect to transistor width (w_{n} and w_{p}).

a) **Computation of rise time and fall time** Breach tool of Matlab provides the function `max_sat_problem = MaxSatProblem(BrSys,phi, params, ranges)`
In the above function BrSys is the object which includes the model and phi is the STL property that is applied on the model. The parameter which has to be optimized is set in to ranges; for example, here the parameters (params) are the nMOS transistor width (w_{n} (μm)) and pMOS transistor width (w_{p} (μm)).The parameters (w_{n} and w_{p}) are set into a range (ranges) to 1.4 - 2.8 and 2.0 - 4.0 respectively.

The STL properties developed to capture the performance requirements at time t of CMOS inverter are described below.

```
param min_tr = 0.2282e-9,
param max_tr = 0.2350e-9,
param min_tf = 0.2272e-9,
param max_tf = 0.2380e-9,
phitr_lw_ok := riseTime[t] > min_tr
phitr_gr_ok := riseTime[t] < max_tr
phi_tr := (phitr_lw_ok and phitr_gr_ok)
phitr_ok := alw_[0.8e-9, 1e-9] (phi_tr )
```

With respect to Figure 6.1, it may be noted that at 0.8 ns the output of the inverter has risen and stabilised and stay that way until the falling edge of the input signal. Thus in the time interval 0.8-1 ns it is checked whether phi_tr is satisfied (i.e. min_tr<risetime<max_tr).

```
phitf_lw_ok := fallTime[t] > min_tf
phitf_gr_ok := fallTime[t] < max_tf
phi_tf := (phitf_lw_ok and phitf_gr_ok)
phitf_ok := alw_[0.8e-9, 1e-9]( phi_tf)
```

With respect to Figure 6.1, it may be noted that at 0.8 ns the output of the inverter has fallen and stabilised and stay that way until the falling edge of the input signal. Thus in the time interval 0.8-1 ns it is checked whether phi_tf is satisfied (i.e. min_tf<falltime<max_tf).

```
alw_phi := alw_[0, 1e-9](phitr_ok and phitf_ok)
```

b) **Computation of power dissipation** The STL properties developed to capture the performance requirements at time t of CMOS inverter: are described below.

```
param min_pd = 0.54010e-3,
param max_pd = 0.54021e-3,
phipd_lw_ok := psc[t] > min_pd
phipd_gr_ok := psc[t] < max_pd
phi_pd := (phipd_lw_ok and phipd_gr_ok)
```

`phipd_ok` := `alw_[0.8e-9, 1e-9] (phi_pd )`
In the time interval 0.8-1 ns it is checked whether phi_pd is satisfied (i.e. min_pd<psc[t]<max_pd).

c) **Computation of rise time and fall time and power dissipation**

```
param min_pd = 0.53921e-3,
param max_pd = 0.54151e-3,
param min_tr = 0.2282e-9,
param max_tr = 0.2350e-9,
param min_tf = 0.2272e-9,
param max_tf = 0.2380e-9,
phitr_lw_ok := riseTime[t] > min_tr
phitr_gr_ok := riseTime[t] < max_tr
phi_tr := (phitr_lw_ok and phitr_gr_ok)
phitr_ok := alw_[0.8e-9, 1e-9] (phi_tr )
```

In the time interval 0.8-1 ns it is checked whether phi_tr is satisfied (i.e. min_tf<risetime<max_tf).

```
phitf_lw_ok := fallTime[t] > min_tf
phitf_gr_ok := fallTime[t] < max_tf
phi_tf := (phitf_lw_ok and phitf_gr_ok)
phitf_ok := alw_[0.8e-9, 1e-9]( phi_tf)
```

In the time interval 0.8-1 ns it is checked whether phi_tf is satisfied (i.e. min_tf<falltime<max_tf).

```
phipd_lw_ok := psc[t] > min_pd
phipd_gr_ok := psc[t] < max_pd
phi_pd := (phipd_lw_ok and phipd_gr_ok)
phipd_ok := alw_[0.8e-9, 1e-9] (phi_pd )
```

In the time interval 0.8-1 ns it is checked whether phi_pd is satisfied (i.e. min_pd<psc[t]<max_pd).

```
alw_phi := alw_[0, 1e-9](phitr_ok and phitf_ok and phipd_ok)
```

5.3 Summary

In this chapter, STL properties for time properties of signals, supported by Breach tool have been used to determine the parameters (transistor size) of the model to achieve different performance goals. Considering the channel length of all transistors to be fixed. Only the transistor width is optimized such that minimum rise time, minimum fall time and minimum power are achieved. Two optimisation algorithms have been used namely Nelder mead

algorithm of Breach tool and a 2D search algorithm. These algorithms are developed such that STL formula captures desired properties (rise time, fall time and power). With increase in transistor width the rise time and fall time decreases. So to achieve minimum rise time and fall time, the optimisation algorithms search for optimal pMOS transistor width and nMOS transistor width. With increase in power, transistor width also increases. To achieve minimum power dissipation, optimisation algorithms searches for optimal pMOS transistor width and nMOS transistor width. In the next chapter, the experimental results have been presented.

Chapter 6

Case Study for CMOS Circuits

In the previous chapter, algorithms for optimizing transistor parameter has been explained. In this chapter, experimental results obtained from the algorithms has been presented here. The rise time and fall time and power dissipation result of CMOS circuits has been tabulated. From the Table 6.1, we find that the computation time for 2D search algorithm is much less as compared to Nelder-Mead algorithm.

Algorithm	**Computation**	**Time (sec)**
2D algo	Rise time and fall time	185.47
	Power (mW)	167.38
	Rise time and fall time and power	221.95
Nelder Mead algo	Rise time and fall time	329.67
	Power (mW)	334.67
	Rise time and fall time and power	329.67

Table 6.1: Compuation time

6.1 Experimental Results for CMOS Inverter

Two different design cases are considered, firstly, achieving desired rise time (t_{r}) and fall time (t_{f}) of the output voltage and secondly, achieving desired power dissipation for given rise time and fall time. Ten different ranges of pMOS transistor width between 2.0 and 4.0 and nMOS transistor width ranging between 1.4 and 2.8 are considered in the study. Using Level 2 technology parameters [83], for 0.35 μm inputs are set as V_{dd} = 3.3 V, k_{n} = 4.9190e-5 A/V^2, k_{p} = 1.7310e-5 A/V^2. Using NM algorithm, the Breach

tool is able to find transistor widths w_n and w_p to satisfy the STL property. Using Figure 6.1 shows the output of CMOS inverter for C_{L} = 50fF. Results for computation of rise time and fall time with load capacitance C_{L} = 50 fF are tabulated in Table 6.2 for ten sets of rise and fall times. The presented two dimensional search algorithm estimates the range of nMOS transistor width (w_n) and pMOS transistor width (w_p) for the STL property. For minimization of power, ranges of transistor widths are determined using NM algorithm and presented 2D search algorithm for the STL property as tabulated in Table 6.3. Table 6.4 tabulates the results for computation of rise time and fall time along with power. NM algorithm estimates a single value of transistor widths for the STL property. Presented 2D search algorithm estimates the range of transistor widths for the STL property. From the results, it has been observed that the transistor width obtained from NM algorithm is within the range obtained from presented 2D search. Execution of NM algorithm and the proposed 2D algorithm results in the minimum error as compared to RGA and DE algorithm [60].

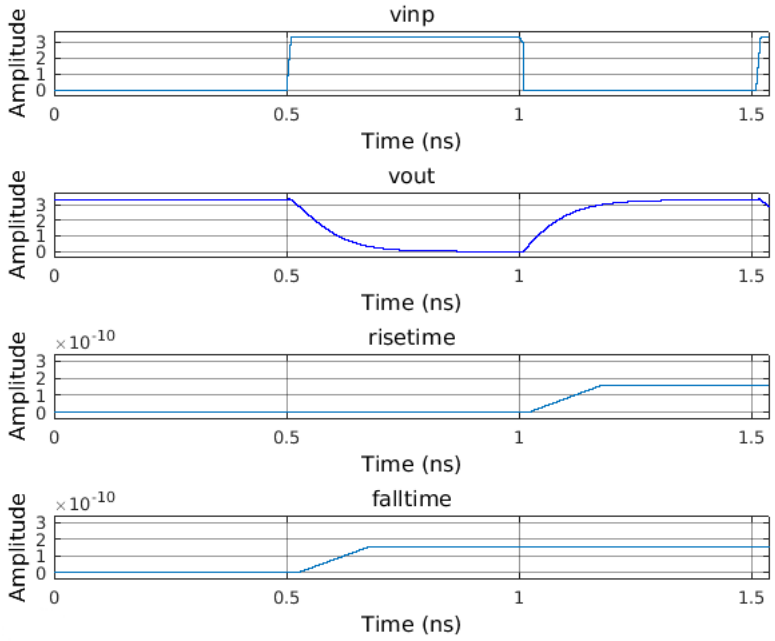


Figure 6.1: Output of CMOS inverter (0.35 μm, V_{dd} = 3.3 V).

Sl	STL property			Nelder Mead algorithm				2D search algorithm	
	$t_{\mathbf{r}}$(ns)	$t_{\mathbf{f}}$(ns)	w_P (μm)	w_N (μm)	$t_{\mathbf{r}}$ (ns)	$t_{\mathbf{f}}$ (ns)	error (ns)	w_P (μm)	w_N (μm)
1	0.2690-0.2710	0.2690-0.2710	2.0001	1.4032	0.2702	0.2700	0.0002	2.0067-2.0130	1.4027- 1.4049
2	0.2345-0.2580	0.2365-0.2535	2.2032	1.5492	0.2450	0.2446	0.0004	2.2005-2.2006	1.5756 -1.6106
3	0.2282-0.2350	0.2272-0.2380	2.3251	1.6501	0.2332	0.2305	0.0027	2.2006-2.3006	1.6456- 1.6675
4	0.2000-0.2280	0.1995-0.2270	2.5157	1.7719	0.2137	0.2153	0.0016	2.3756-2.6407	1.6718- 1.8907
5	0.1800-0.2000	0.1805-0.1995	2.8412	1.9933	0.1904	0.1893	0.0011	2.7607-2.9527	1.9747- 2.0419
6	0.1667-0.1800	0.1667-0.1805	3.1154	2.1893	0.1734	0.1732	0.0002	3.1688-3.1688	2.2688 -2.3192
7	0.1572-0.1637	0.1556-0.1648	3.3655	2.3623	0.1603	0.1604	0.0001	3.1688-3.3129	2.3696- 2.4205
8	0.1543-0.1570	0.1517-0.1555	3.4672	2.4769	0.1555	0.1532	0.0023	3.5001-3.5865	2.4352 -2.4427
9	0.1400-0.1458	0.1400-0.1460	3.7704	2.6451	0.1435	0.1433	0.0002	3.6297 -3.8125	2.6923 -2.7831
10	0.1354-0.1400	0.1350-0.1400	3.9223	2.7607	0.1375	0.1376	0.0001	3.6297 -3.9754	2.7982 -2.8436

Table 6.2: Results of CMOS inverter for rise time and fall time computation (0.35 μm, $V_{\mathrm{dd}} = 3.3$ V)

Sl	STL property	Nelder Mead algorithm		2D search algorithm	
	$p_{\mathbf{sc}}$(mW)	w_P (μm)	w_N (μm)	w_P (μm)	w_N (μm)
1	0.53640 - 0.53801	2.0741	1.4558	1.9171 - 2.2005	1.3713 - 1.6106
2	0.53820 - 0.54001	2.2006	1.4563	2.2005 - 2.3006	1.6106 - 1.6456
3	0.54010 - 0.54021	2.3055	1.6894	2.3506 - 2.3756	1.6631 - 1.6718
4	0.54031 - 0.54121	2.3901	1.7919	2.3756 - 2.7607	1.6718 - 1.9747
5	0.54125 - 0.54141	2.4697	1.9515	2.7607 - 3.1688	1.9747 - 2.3192
6	0.54227 - 0.54290	2.8148	2.3709	2.7047 - 2.8829	1.9035- 2.0175
7	0.54151 - 0.54241	2.6009	2.1875	3.1688 - 3.1688	2.3192 - 2.3192
8	0.54291 - 0.54310	3.0112	2.4937	3.3848 - 3.4388	2.3948 - 2.4138
9	0.54312 - 0.54330	3.1089	2.6351	3.3848 - 3.4388	2.3948 - 2.4138
10	0.54320 - 0.54360	3.1979	2.7410	3.8025 - 3.8025	2.7831 - 2.7831

Table 6.3: Results of CMOS inverter for power computation (0.35 μm, V_{dd} = 3.3 V)

6.2 Experimental Result for CMOS NAND2

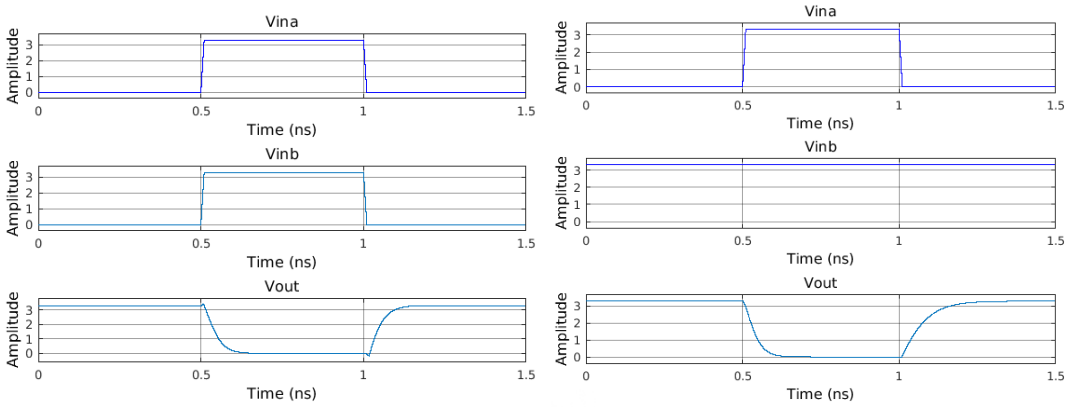
The sizes of both the pMOS transistors and nMOS transistors are symmetric. Two different design cases are considered, firstly, achieving desired rise time (t_{r}) and fall time (t_{f}) of the output voltage and secondly, achieving desired power dissipation for given rise time and fall time. Ten different ranges of pMOS transistor width between 2.0 and 4.0 and nMOS transistor width ranging between 1.4 and 2.8 are considered in the study. Using Level 2 technology parameters, for 0.35 μm inputs are set as V_{dd} = 3.3 V, k_{n} = 4.9190e-5 A/V^2, k_{p} = 1.7310e-5 A/V^2. Results for computation of rise time and fall time with load capacitance C_{L} = 50 fF are tabulated in Table 6.5 for ten sets. Using NM algorithm, the Breach tool is able to find transistor widths w_n and w_p to satisfy the STL property. Figure 6.2 shows the output of CMOS NAND2 for C_{L} = 50 fF. The presented 2D search algorithm estimates the range of nMOS transistor width (w_n) and pMOS transistor width (w_p) for the ten sets of STL property. For minimization of power, transistor widths are determined using NM algorithm and presented 2D search algorithm for the STL property as tabulated in Table 6.6. NM algorithm estimates a single value of transistor widths for a STL property. The results for computation of rise time and fall time along with power are tabulated in Table 6.7.

Sl	STL property			Nelder Mead algorithm					2D search algorithm			
	t_r(ns)	t_f(ns)	p_{sc} (mW)	w_P (μm)	w_N (μm)	p_p(mW)	p_n (mW)	w_P (μm)	w_N (μm)	p_p (mW)	p_n (mW)
1	0.2690-0.2710	0.2690-0.2710	0.53640-0.54031	2.0001	1.4067	8.433	8.151	2.0001-2.0149	1.4040-1.4139	8.2007 - 8.1356	8.4952 - 8.4328
2	0.2345-0.2580	0.2365-0.2535	0.53640-0.54031	2.2775	1.5897	9.602	9.326	2.0933-2.3027	1.4951-1.6034	9.4114 - 8.7083	9.7086 - 8.8256
3	0.2282-0.2350	0.2272-0.2380	0.53921-0.54151	2.3301	1.6217	9.824	9.528	2.2979-2.3665	1.5929-1.6689	9.8184 - 9.3496	9.9775 - 9.6880
4	0.2000-0.2280	0.1995-0.2270	0.54031-0.54260	2.4610	1.7820	10.375	10.511	2.3683-2.6999	1.6702-1.9003	11.254 - 9.8246	11.383 - 9.9851
5	0.1800-0.2000	0.1805-0.1995	0.54031-0.54305	2.7997	1.9609	11.804	11.623	2.7071-3.0003	1.9002-2.1065	12.523 - 11.254	12.649 - 11.413
6	0.1667-0.1800	0.1667-0.1805	0.54151-0.54323	3.0078	2.2508	12.681	13.399	3.0000-3.2399	2.1001-2.2740	13.545 - 12.485	13.659 - 12.648
7	0.1572-0.1637	0.1556-0.1648	0.54305-0.54330	3.4093	2.3052	14.374	13.735	3.2991-3.4355	2.3009-2.4366	14.539 - 13.710	14.484 - 13.909
8	0.1543-0.1570	0.1517-0.1555	0.54320-0.54360	3.4495	2.4941	14.543	14.895	3.4676-3.5001	2.4238-2.4503	14.928 - 14.550	14.756 - 14.503
9	0.1400-0.1458	0.1400-0.1460	0.54323-0.54360	3.9499	2.7856	16.653	16.678	3.7045-3.8577	2.5967-2.7079	16.197 - 15.516	16.263 - 15.618
10	0.1354-0.1400	0.1350-0.1400	0.54323-0.54360	3.9741	2.7932	16.755	16.724	3.8577-3.9885	2.7079-2.8085	16.818 - 16.197	16.815 - 16.264

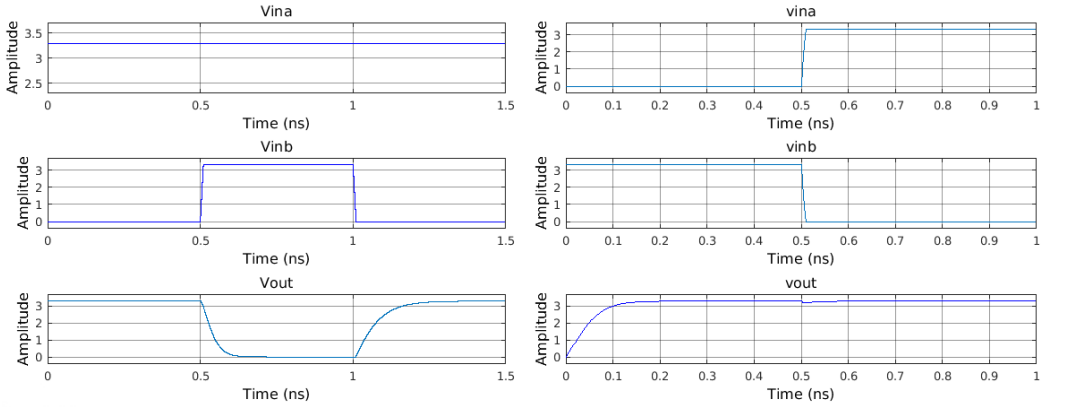
Table 6.4: Results of CMOS inverter for rise time and fall time and power computation (0.35 μm, $V_{dd} = 3.3$ V)

Sl	STL property		Nelder Mead algorithm					2D search algorithm	
	$t_{\mathbf{r}}$(ns)	$t_{\mathbf{f}}$(ns)	w_P (μm)	w_N (μm)	$t_{\mathbf{r}}$ (ns)	$t_{\mathbf{f}}$ (ns)	error (ns)	w_P (μm)	w_N (μm)
1	0.13100 - 0.13500	0.13100 - 0.13600	2.0296	1.4187	0.13304	0.13360	0.0005	2.0003 - 2.0505	1.4004-1.4180
2	0.12860 - 0.13050	0.12640 - 0.13050	2.0815	1.4781	0.12973	0.12825	0.0014	2.0505- 2.2005	1.4180-1.6106
3	0.11740 - 0.12860	0.11850 - 0.12640	2.1444	1.5375	0.12592	0.12330	0.0026	2.2005- 2.2005	1.5756-1.6106
4	0.10000 - 0.11740	0.09970 - 0.11850	2.4481	1.6937	0.11030	0.11192	0.0016	2.6407- 2.3006	1.6456-1.8907
5	0.09001 - 0.10000	0.09027 - 0.09970	2.8111	1.9625	0.09606	0.09659	0.0005	2.7607- 2.9527	1.9747-2.0419
6	0.08550 - 0.09005	0.08550 - 0.09030	3.0667	2.1750	0.08805	0.08716	0.0008	3.0247- 3.1688	2.0671-2.3192
7	0.07998 - 0.08185	0.07992 - 0.08245	3.3296	2.3375	0.08110	0.08109	0.0001	2.9167- 3.3128	2.3696-2.3712
8	0.07714 - 0.07998	0.07582 - 0.07992	3.4407	2.4625	0.07848	0.07698	0.0014	3.3848- 3.5001	2.3948-2.4352
9	0.07001 - 0.07292	0.07001 - 0.07300	3.7444	2.6375	0.07212	0.07187	0.0002	3.6297- 3.8025	2.6923-2.7832
10	0.06750 - 0.06950	0.06700 - 0.06970	3.9111	2.7625	0.06904	0.06862	0.0004	3.8025- 3.9754	2.8133-2.8436

Table 6.5: Results of CMOS NAND2 for rise time and fall time computation (0.35 μm, $V_{\mathrm{dd}} = 3.3$ V)



(a) $V_{\text{inA}} = V_{\text{inB}} = 0 \rightarrow 1$ (b) $V_{\text{inA}} = 0 \rightarrow 1$, $V_{\text{inB}} = 1$



(c) $V_{\text{inA}} = 1$, $V_{\text{inB}} = 0 \rightarrow 1$ (d) $V_{\text{inA}} = 0 \rightarrow 1$, $V_{\text{inB}} = 1 \rightarrow 0$

Figure 6.2: Output of CMOS NAND2 (0.35 μm, $V_{\text{dd}} = 3.3$ V).

6.3 Experimental Result for CMOS NOR2

Similarly for CMOS NOR2, two different design cases are considered, firstly, achieving desired rise time (t_{r}) and fall time (t_{f}) of the output voltage and secondly, achieving desired power dissipation for given rise time and fall time. The size of both the pMOS transistors and both the nMOS transistors are symmetric. Ten different ranges of pMOS transistor width between 2.0 and 4.0 and nMOS transistor width ranging between 1.4 and 2.8 are considered in the study. Using Level 2 technology parameters, for 0.35 μm inputs are set as $V_{\text{dd}} = 3.3$ V, $k_{\text{n}} = 4.9190\text{e-}5\ A/V^2$, $k_{\text{p}} = 1.7310\text{e-}5\ A/V^2$. Using NM algorithm, the Breach tool is able to find transistor widths w_n and w_p to satisfy the STL property. Figure 6.3 shows the output of CMOS NOR2 for C_{L} =50 fF. The results for computation of rise time and fall time with load

Sl	STL property	Nelder Mead algorithm		2D search algorithm	
	$p_{\mathbf{sc}}$(mW)	w_P (μm)	w_N (μm)	w_P (μm)	w_N (μm)
1	0.27182-0.27193	1.4923	2.8975	1.9901-1.9901	1.3968-1.3968
2	0.27180- 0.27190	1.5370	2.8975	1.9901-1.9901	1.3968-1.3968
3	0.27177- 0.27187	1.6937	3.0590	1.9901-1.9901	1.3968-1.3968
4	0.27170- 0.27180	1.9620	3.1204	1.9901-1.9901	1.3968-1.3968
5	0.27170- 0.27155	2.1750	3.2511	1.8336-1.8336	1.1656-1.3421
6	0.27162- 0.27167	2.2625	3.3036	1.6627-1.8336	1.1549-1.1656
7	0.27152- 0.27167	2.3375	3.4804	1.6323-1.6323	1.1549-1.1549
8	0.27132 -0.27157	2.4625	3.5882	1.6323-1.6323	1.1549-1.1549
9	0.27166- 0.27168	2.6375	3.7439	1.5976-1.5976	1.1428-1.1428
10	0.27163 -0.27165	2.7625	3.7439	1.5976-1.5976	1.1428-1.1428

Table 6.6: Results of CMOS NAND2 for computaion of power (0.35 μm, $V_{\rm dd} = 3.3$ V)

capacitance $C_{\rm L} = 50$ fF for the STL property are tabulated in Table 6.8. The presented 2D search algorithm estimates the range of nMOS transistor width (w_n) and pMOS transistor width (w_p) for the STL property. NM algorithm estimates a single value of transistor sizing for a STL property. For minimization of power, transistor widths are determined using NM algorithm and presented 2D search algorithm for the STL property as tabulated in Table 6.9. The results for computation of rise time and fall time along with power for the STL property are tabulated in Table 6.10.

6.4 Experimental Result for Secure Circuit

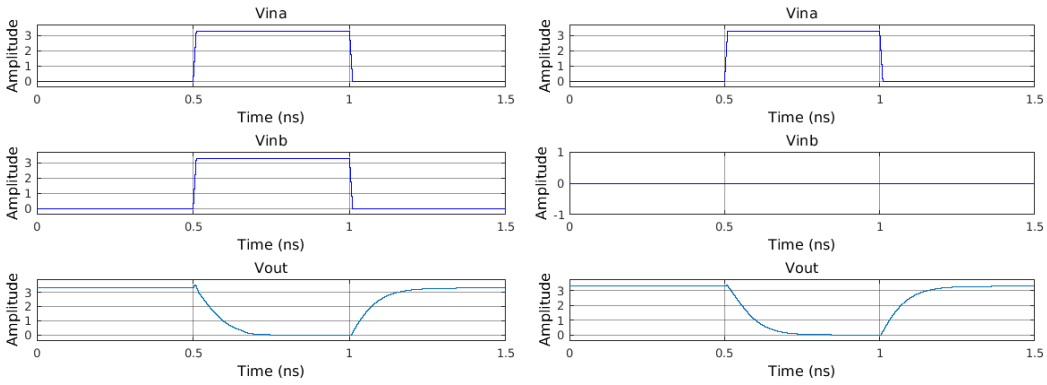
Two different design cases are considered, firstly, achieving desired rise time ($t_{\rm r}$) and fall time ($t_{\rm f}$) of the output voltage and secondly, achieving desired power dissipation for given rise time and fall time. Ten different ranges of pMOS transistor width between 1.8 and 3.6 and nMOS transistor width ranging between 0.9 and 1.8 are considered in the study. Using BSIM3 Level 49 technology parameters [73], for 0.18 μm inputs are set as $V_{\rm dd} = 1.8$ V. Using NM algorithm, the Breach tool is able to find transistor widths w_n and w_p to satisfy the STL property. Using Figure 6.4 shows the output of secure circuit for $C_{\rm L} = 20$fF. Results for computation of rise time and fall time with load capacitance $C_{\rm L} = 20$ fF are tabulated in Table 6.11 and Table 6.20 for ten sets of rise and fall times. The average power (pavg(μW)) is 0.9 μW and PPV is 0.176 μ_W. The presented two dimensional search algorithm estimates

Sl	STL property			Nelder Mead algorithm				2D search algorithm			
	$t_{\mathbf{r}}$(ns)	$t_{\mathbf{f}}$(ns)	$p_{\mathbf{sc}}$(mW)	w_{P} (μm)	w_{N} (μm)	$p_{\mathbf{p}}$(mW)	$p_{\mathbf{n}}$ (mW)	w_{P} (μm)	w_{N} (μm)	$p_{\mathbf{p}}$ (mW)	$p_{\mathbf{n}}$ (mW)
1	0.1310-0.1350	0.1310-0.1360	0.27182- 0.27193	2.0296	1.4187	17.122	16.615	2.0002- 2.0611	1.3937-1.4473	17.388 - 16.874	16.95 - 16.322
2	0.1286-0.1305	0.1264-0.1305	0.27180- 0.27190	2.0827	1.4801	17.571	17.335	2.0689- 2.1001	1.4527- 1.4998	17.771 - 17.454	17.566 - 17.013
3	0.1174-0.1286	0.1185-0.1264	0.27177- 0.27187	2.1124	1.4890	17.821	17.438	2.0995- 2.3003	1.5000- 1.5998	19.406 - 17.712	18.729 - 17.569
4	0.1000-0.1174	0.0997-0.1185	0.27170- 0.27180	2.1419	1.4831	18.070	17.366	2.3001- 2.6999	1.5997- 1.9015	22.778 - 19.405	22.252 - 18.728
5	0.0900-0.1000	0.0902-0.0997	0.27179 -0.27182	2.0790	2.2209	17.539	26.134	2.7001- 2.9998	1.9016- 2.0998	25.308 - 22.779	24.561 - 22.253
6	0.0855-0.0900	0.0855-0.0903	0.27176 -0.27179	2.0741	2.1875	17.497	25.736	2.9990- 3.1584	2.0995- 2.2174	26.646 - 25.301	25.933 - 24.557
7	0.0799-0.0818	0.0799-0.0824	0.27173 -0.27175	2.0741	2.1875	17.497	25.736	3.2991- 3.3762	2.2994- 2.3719	28.483 - 27.833	27.734 - 26.884
8	0.0771-0.0799	0.0758-0.0799	0.27171- 0.27173	2.0790	2.2209	17.539	26.134	3.3762- 3.5006	2.3719- 2.5004	29.533 - 28.483	29.241 - 27.734
9	0.0700-0.0729	0.0700-0.0730	0.27166- 0.27168	2.0934	2.1965	17.660	25.840	3.7030- 3.8569	2.7079 - 2.5967	32.539 - 31.240	31.649 - 30.352
10	0.0675-0.0695	0.0670-0.0697	0.27163- 0.27165	2.0790	2.2209	17.539	26.134	3.8852- 4.0008	2.8293 - 2.7196	33.752 - 32.777	33.07 - 31.783

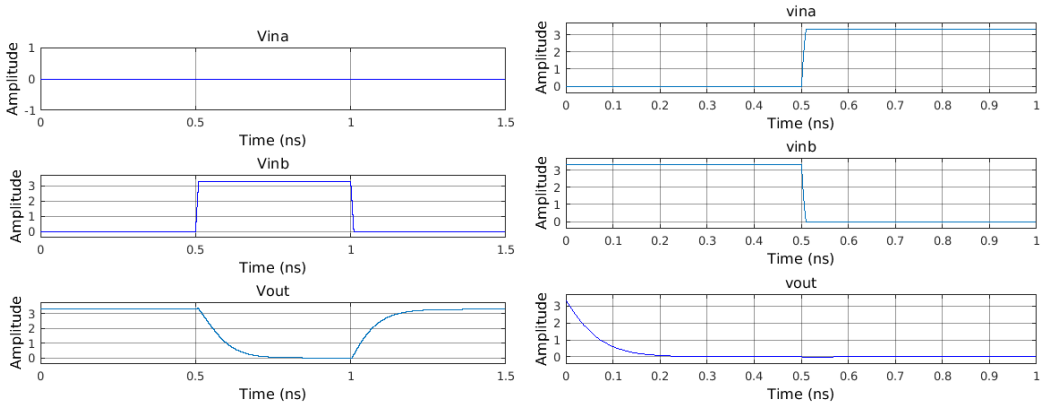
Table 6.7: Results of CMOS NAND2 for rise time and fall time and power computation (0.35 μm, $V_{\mathrm{dd}} = 3.3$ V)

Sl	STL property		Nelder Mead algorithm					2D search algorithm	
	$t_{\mathbf{r}}$(ns)	$t_{\mathbf{f}}$(ns)	w_P (μm)	w_N (μm)	$t_{\mathbf{r}}$ (ns)	$t_{\mathbf{f}}$ (ns)	error (ns)	w_P (μm)	w_N (μm)
1	0.2690-0.2710	0.2690-0.2710	2.0370	1.4312	0.26510	0.26490	0.0002	1.6670-2.0067	1.4005-1.4027
2	0.2345-0.2580	0.2365-0.2535	2.1963	1.5687	0.24590	0.24160	0.0043	2.0067-2.0130	1.4027-1.4049
3	0.2282-0.2350	0.2272-0.2380	2.3296	1.6844	0.23180	0.22500	0.0068	2.0005-2.2005	1.5756-1.6106
4	0.2000-0.2280	0.1995-0.2270	2.4926	1.8062	0.21667	0.20990	0.0067	2.2005 -2.3006	1.6456-1.6675
5	0.1800-2.0000	0.1805-0.1995	2.8111	1.9625	0.19212	0.19319	0.0010	2.3756-2.6407	1.6718-1.8907
6	0.1667-0.1800	0.1667-0.1805	3.1111	2.1625	0.17359	0.17532	0.0017	2.7607-2.9527	1.9747-2.0419
7	0.1572-0.1637	0.1556-0.1648	3.3741	2.3625	0.16006	0.16048	0.0004	3.1688 -3.1688	2.2688- 2.3192
8	0.1543-0.1570	0.1517-0.1555	3.4407	2.4625	0.15696	0.15396	0.0030	3.1688 -3.3128	2.2688-2.3696
9	0.1400-0.1460	0.1400-0.1458	3.7667	2.6750	0.14338	0.14173	0.0016	3.1688 -3.3128	2.3696-2.4201
10	0.1350-0.1400	0.1350-0.1400	3.9111	2.7625	0.13808	0.13724	0.0008	3.6297 -3.8025	2.6923-2.7831

Table 6.8: Results of CMOS NOR2 for rise time and fall time computation (0.35 μm, $V_{\mathrm{dd}} = 3.3$ V)



(a) $V_{\text{inA}} = V_{\text{inB}} = 0 \rightarrow 1$ (b) $V_{\text{inA}} = 0 \rightarrow 1$, $V_{\text{inB}} = 0$



(c) $V_{\text{inA}} = 0$, $V_{\text{inB}} = 0 \rightarrow 1$ (d) $V_{\text{inA}} = 0 \rightarrow 1$, $V_{\text{inB}} = 1 \rightarrow 0$

Figure 6.3: Output of CMOS NOR2 (0.35 μm, $V_{\text{dd}} = 3.3$ V).

the range of nMOS transistor width (w_n) and pMOS transistor width (w_p) for the STL property.

6.5 Validation of CMOS Circuits

In order to verify the results achieved through the NM algorithm and proposed 2D search algorithm, the CMOS circuits has been redesigned with synthesized values of output load capacitance and transistor size using Spice simulator. Spice vs NM results of CMOS inverter for rise time and fall time computation is tablulated in Table 6.13 and Table 6.14 show the spice vs 2D search results.

Sl	STL property	Nelder Mead algorithm		2D search algorithm	
	$p_{\mathbf{sc}}$(mW)	w_P (μm)	w_N (μm)	w_P (μm)	w_N (μm)
1	0.53640-0.53801	2.0740	1.4000	1.9979 - 2.2005	1.3996 - 1.6106
2	0.53820-0.54001	2.2222	1.6625	2.2005 - 2.2005	1.6106 - 1.6106
3	0.54010-0.54021	2.2963	1.6625	2.2005 - 2.2005	1.6106 - 1.6106
4	0.54125-0.54141	2.4444	1.9250	2.3006 - 2.3506	1.6456 - 1.6631
5	0.54151-0.54241	2.7407	1.8375	2.3756 - 2.6407	1.6718 - 1.9327
6	0.54251-0.54303	2.8888	2.4937	2.6407 - 2.6407	1.9327 - 1.9327
7	0.54285-0.54330	2.8888	2.3625	2.7607 - 2.7607	1.9747 - 1.9747
8	0.54285-0.54330	2.8888	2.3625	3.1688 - 3.3848	2.3192 - 2.3948
9	0.54285-0.54330	2.8888	2.3625	3.3848 - 3.3848	2.3948 - 2.3948
10	0.54285-0.54330	2.8888	2.3625	3.3848 - 3.3848	2.3948 - 2.3948

Table 6.9: Results of CMOS NOR2 for power computation (0.35 μm, V_{dd} = 3.3 V)

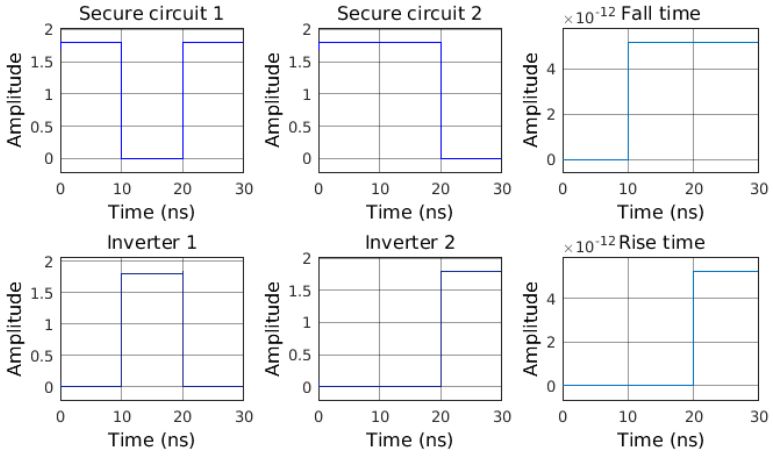


Figure 6.4: Output of Secure circuit (180 nm, V_{dd} = 1.8 V).

Sl	STL property			Nelder Mead algorithm				2D search algorithm			
	t_r(ns)	t_f(ns)	p_{sc}(mW)	w_P (μm)	w_N (μm)	p_p(mW)	p_n (mW)	w_P (μm)	w_N (μm)	p_p (mW)	p_n(mW)
1	0.2690-0.2710	0.2690-0.2710	0.53640-0.53801	2.0000	1.4000	16.873	16.513	1.9930- 2.0079	1.3991- 1.4094	16.939 - 16.814	16.657 - 16.514
2	0.2345-0.2580	0.2365-0.2535	0.53820-0.54001	2.2963	1.6625	19.332	19.994	2.0002- 2.0149	1.4040-1.4133	16.999 - 16.874	16.712 - 16.581
3	0.2282-0.2350	0.2272-0.2380	0.54010-0.54021	2.2963	1.6625	19.337	19.994	2.0931- 2.3033	1.4954- 1.6031	19.431 - 17.658	19.253 - 17.786
4	0.2000-0.2280	0.1995-0.2270	0.54125-0.54141	2.4440	1.9250	23.396	20.618	2.2978- 2.3666	1.5928- 1.6688	19.996 - 19.385	20.113 - 19.126
5	0.1800-2.000	0.1805-0.1995	0.54151-0.54241	2.7407	1.8375	23.122	22.357	2.3689- 2.7002	1.6705- 1.9002	22.780 - 19.985	23.154 - 20.129
6	0.1667-0.1800	0.1667-0.1805	0.54251-0.54303	2.8148	2.4937	23.747	30.978	2.7002- 2.9918	1.8982- 2.1006	25.240 - 22.780	25.798 - 23.129
7	0.1572-0.1637	0.1556-0.1648	0.54285-0.54330	2.9629	2.3625	24.997	29.233	3.0003- 3.2388	2.1006- 2.2747	27.324 - 25.311	28.095 - 25.798
8	0.1543-0.1570	0.1517-0.1555	0.54285-0.54330	2.9629	2.3625	24.997	29.233	3.2473- 3.2979	2.2771- 2.3007	27.822 - 27.395	28.428 - 28.127
9	0.1400-0.1460	0.1400-0.1458	0.54285-0.54330	2.9629	2.3625	24.997	29.233	3.2990- 3.4358	2.3007- 2.4366	28.985 - 27.832	30.247 - 28.440
10	0.1350-0.1400	0.1350-0.1400	0.54285-0.54330	2.9629	2.3625	24.997	29.233	3.6989- 3.8576	2.5964- 2.7079	32.544 - 31.205	33.891 -32.385

Table 6.10: Results of CMOS NOR2 for rise time and fall time and power computation (0.35 μm, $V_{dd} = 3.3$ V)

Sl No.	Nelder Mead Algorithm						
	tr(ps)	tf(ps)	weffp(um)	weffn(um)	tr(ps)	tf(ps)	error(ps)
1	10.320-10.460	1.030-10.400	1.8	0.9	10.420	10.340	0.0800
2	9.3666-9.3686	9.3000-9.3015	1.9805	1.0345	9.3676	9.3005	0.0671
3	8.9570-8.9580	8.8925-8.8945	2.0046	1.0458	8.9577	8.8935	0.0641
4	8.5005-8.5250	8.4500-8.4650	2.2005	1.1678	8.5160	8.8455	0.0610
5	7.8060-7.8075	7.7500-7.7510	2.4479	1.2587	7.8063	7.7504	0.0559
6	7.2050-7.2065	7.1532-7.1552	2.6257	1.3346	7.2056	7.1542	0.0516
7	6.2400-6.2550	6.2000-6.2015	3.1347	1.5709	6.2450	6.2003	0.0447
8	5.8537-5.8556	5.8120-5.8130	3.4223	1.6345	5.8547	5.8128	0.0419
9	5.5100-5.5115	5.4700-5.4715	3.4356	1.7356	5.5103	5.4709	0.0395
10	5.2000-5.2150	5.1650-5.1750	3.6	1.8	5.2090	5.1710	0.0380

Table 6.11: Results of CMOS secure circuit for rise time and fall time computation (180 nm, $V_{\text{dd}} = 1.8$ V)

6.6 Summary

Successful experimentation on CMOS inverter, NAND2 and NOR2 gates and precharge based circuit have been done. Using NM algorithm for minimum rise time, minimum fall time and minimum power dissipation, a single pMOS transistor width and nMOS transistor width is achieved. But using presented 2D search algorithm, a range of admissible parameters is obtained. The CMOS circuits has been redisgned using Spice simulator with synthesized values of transistor size obtained using optimisation algorithms. Results obtained from NM and 2D search algorithm are comparable with the Spice.

Sl No.	STL property		2D search algorithm				
	tr(ps)	tf(ps)	weffp(um)	weffn(um)	tr(ps)	tf(ps)	error(ps)
1	10.10-10.50	10.10 -10.50	1.781745-1.8005	0.89581-0.99055	10.457-9.4569	10.382-9.3892	0.0749-0.0677
2	9.3676-9.4676	9.3005-9.4005	1.98055-1.98055	0.945525-1.035575	9.9073-9.0458	9.8363-8.9810	0.0710-0.0648
3	8.9760-9.2760	8.9500-9.2500	1.890525-2.070575	1.001806-1.058088	9.3507-8.8533	9.2837-8.7899	0.0670-0.0634
4	8.6750-8.875	8.6700-8.8700	1.98055-2.138094	1.046831-1.074972	8.9485-8.7142	8.8844-8.6518	0.0641-0.0624
5	8.4516-8.650	8.455-8.6200	2.167352-2.1606	1.082288-1.18866	8.6553-7.8808	8.5933-7.8243	0.0620-0.0565
6	7.2056-7.4056	7.1542-7.4542	2.37666-2.59272	1.256198-1.426392	7.4571-6.5673	7.4037-6.5203	0.0534-0.0471
7	6.245-6.5450	6.2003-6.5003	2.625129-2.981628	1.430444-1.523646	6.5487-6.1481	6.5018-6.1041	0.0469-0.0440
8	5.8547-5.9947	5.8128-5.9928	3.130709-3.111264	1.560927-1.71167	6.0013-5.4728	5.9583-5.4336	0.0430-0.0392
9	5.4103-5.6103	5.3709 -5.5709	3.42239-3.42239	1.633867-1.789474	5.7334-5.2348	5.6923-5.1973	0.0411-0.0375
10	5.209-5.4005	5.171-5.3605	3.266827-3.577954	1.731121-1.828375	5.4113-5.1234	5.3725-5.0867	0.0388-0.0367

Table 6.12: Results of CMOS secure circuit for rise time and fall time computation (180 nm, $V_{\mathrm{dd}} = 1.8$ V)

Sl No.	**Spice input**		**Spice result**		**Nelder Mead algorithm**	
	w_P (μm)	w_N (μm)	$t_\mathbf{r}$(ns)	$t_\mathbf{f}$(ns)	$t_\mathbf{r}$(ns)	$t_\mathbf{f}$(ns)
1	2.0001	1.4032	0.2733	0.2732	0.2702	0.2700
2	2.2032	1.5492	0.2611	0.2587	0.2450	0.2446
3	2.3251	1.6501	0.2410	0.2348	0.2332	0.2305
4	2.5157	1.7719	0.2288	0.2411	0.2137	0.2153
5	2.8412	1.9933	0.2065	0.2201	0.1904	0.1893
6	3.1154	2.1893	0.1666	0.1806	0.1734	0.1732
7	3.3655	2.3623	0.1506	0.1688	0.1603	0.1604
8	3.4672	2.4769	0.1465	0.1551	0.1555	0.1532
9	3.7704	2.6451	0.1348	0.1287	0.1435	0.1433
10	3.9223	2.7607	0.1301	0.1290	0.1375	0.1376

Table 6.13: Spice results vs NM results of CMOS inverter for rise time and fall time computation (0.35 μm, $V_{dd} = 3.3$ V)

Sl No.	Spice input		Spice result		2D search algorithm	
	w_P (μm)	w_N (μm)	t_r(ns)	t_f(ns)	t_r (ns)	t_f (ns)
1	2.0130- 2.0067	1.4049- 1.4027	0.2700-0.2689	0.2941-0.2960	0.2686- 0.2691	0.2699- 0.2703
2	2.2005- 2.2005	1.5756- 1.6106	0.2611-0.2611	0.2790-0.2658	0.2454- 0.2454	0.2406- 0.2354
3	2.2005- 2.3006	1.6675 -1.6456	0.2611-0.2405	0.2568-0.2599	0.2454- 0.2346	0.2274- 0.2304
4	2.6407- 2.3756	1.8907- 1.6718	0.2154-0.2389	0.2311-0.2534	0.2045- 0.2273	0.2005- 0.2268
5	2.9527- 2.7607	2.0419- 1.9747	0.1955-0.2005	0.1911-0.2036	0.1829- 0.1956	0.1857- 0.1920
6	3.1688- 3.1688	2.2688- 2.3192	0.1686-0.1686	0.1605-0.1544	0.1704- 0.1704	0.1671- 0.1635
7	3.2688- 3.3129	2.4205- 2.3696	0.1645-0.1532	0.1402-0.1536	0.1704- 0.1630	0.1567- 0.1600
8	3.5001- 3.5865	2.4352- 2.4427	0.1535-0.1559	0.1599-0.1546	0.1543- 0.1562	0.1557- 0.1552
9	3.6297- 3.8125	2.6923- 2.7831	0.1498-0.1321	0.1324-0.1301	0.1488- 0.1420	0.1408- 0.1362
10	3.6297- 3.9754	2.7982- 2.8436	0.1498-0.1278	0.1291-0.1297	0.1488- 0.1359	0.1355- 0.1333

Table 6.14: Spice results vs 2D search results of CMOS inverter for rise time and fall time computation (0.35 μm, $V_{dd} = 3.3$ V)

Sl No.	Spice input		Spice result		Nelder Mead algorithm	
	w_P (μm)	w_N (μm)	t_r(ns)	t_f(ns)	t_r(ns)	t_f(ns)
1	2.0296	1.4187	0.13298	0.13348	0.13304	0.13360
2	2.0815	1.4781	0.12965	0.12803	0.12973	0.12825
3	2.1444	1.5375	0.12589	0.12318	0.12592	0.12330
4	2.4481	1.6937	0.11021	0.11167	0.11030	0.11192
5	2.8111	1.9625	0.09599	0.09649	0.09606	0.09659
6	3.0667	2.1750	0.08789	0.08701	0.08805	0.08716
7	3.3296	2.3375	0.08100	0.08099	0.08110	0.08109
8	3.4407	2.4625	0.07837	0.07688	0.07848	0.07698
9	3.7444	2.6375	0.07200	0.07167	0.07212	0.07187
10	3.9111	2.7625	0.06899	0.06854	0.06904	0.06862

Table 6.15: Spice results vs NM results of CMOS NAND2 for rise time and fall time computation (0.35 μm, $V_{dd} = 3.3$ V)

Sl No.	Spice input		Spice result		2D search algorithm	
	w_P (μm)	w_N (μm)	t_r(ns)	t_f(ns)	t_r(ns)	t_f(ns)
1	2.0003 - 2.0505	1.4004 - 1.4180	0.13529 - 0.13160	0.13487 - 0.13361	0.13536 - 0.13169	0.13499 - 0.13369
2	2.0505 - 2.2005	1.4180 - 1.6106	0.13160 - 0.12267	0.13361 - 0.11763	0.13169 - 0.12271	0.13369 - 0.11770
3	2.2005 - 2.2005	1.5756 - 1.6106	0.12267 - 0.12267	0.12025 - 0.11763	0.12271 - 0.12271	0.12032 - 0.11770
4	2.3006 - 2.6407	1.6456 - 1.8907	0.11731 - 0.10219	0.11509 - 0.10019	0.11738 - 0.10226	0.11520 - 0.10026
5	2.7607 - 2.9527	1.9747 - 2.0419	0.09773 - 0.09138	0.09587 - 0.09277	0.09781 - 0.09145	0.09599 - 0.09284
6	3.0247 - 3.1688	2.0671 - 2.3192	0.08919 - 0.08519	0.09163 - 0.08165	0.08927 - 0.08522	0.09171 - 0.08174
7	2.9167 - 3.3128	2.3696 - 2.3712	0.09249 - 0.08143	0.07987 - 0.07982	0.09258 - 0.08151	0.07999 - 0.07994
8	3.3848 - 3.5001	2.4352 - 2.3948	0.07973 - 0.07168	0.07777 - 0.07908	0.07978 - 0.07175	0.07784 - 0.07916
9	3.6297 - 3.8025	2.6923 - 2.7832	0.07491 - 0.07082	0.07033 - 0.06801	0.07439 - 0.07101	0.07041 - 0.06811
10	3.8025 - 3.9754	2.8133 - 2.8436	0.07082 - 0.06783	0.06729 - 0.06659	0.07101 - 0.06792	0.06738 - 0.06666

Table 6.16: Spice results vs 2D search results of CMOS NAND2 for rise time and fall time computation (0.35 μm, $V_{dd} = 3.3$ V)

Sl No.	**Spice input**		**Spice result**		**Nelder Mead algorithm**	
	w_P (μm)	w_N (μm)	$t_\mathbf{r}$(ns)	$t_\mathbf{f}$(ns)	$t_\mathbf{r}$(ns)	$t_\mathbf{f}$(ns)
1	2.0370	1.4312	0.26500	0.26478	0.26510	0.26490
2	2.1963	1.5687	0.24583	0.24156	0.24590	0.24160
3	2.3296	1.6844	0.23168	0.22500	0.23180	0.22500
4	2.4926	1.8062	0.21657	0.20982	0.21667	0.20990
5	2.8111	1.9625	0.19201	0.19300	0.19212	0.19319
6	3.1111	2.1625	0.17347	0.17521	0.17359	0.17532
7	3.3741	2.3625	0.16000	0.16042	0.16006	0.16048
8	3.4407	2.4625	0.15687	0.15388	0.15696	0.15396
9	3.7667	2.6750	0.14330	0.14168	0.14338	0.14173
10	3.9111	2.7625	0.13797	0.13712	0.13808	0.13724

Table 6.17: Spice results vs Nelder mead results of CMOS NOR2 for rise time and fall time computation (0.35 μm, $V_{\rm dd} = 3.3$ V)

Sl No.	Spice input		Spice result		2D search algorithm	
	w_P (μm)	w_N (μm)	t_r(ns)	t_f(ns)	t_r(ns)	t_f(ns)
1	1.6671 - 2.0067	1.4005 - 1.4027	0.32209 - 0.26900	0.27067 - 0.27010	0.32390- 0.26912	0.27072 - 0.27029
2	2.0067 - 2.0130	1.4027 - 1.4049	0.26900 - 0.26819	0.27010 - 0.26973	0.26912 - 0.26829	0.27029 - 0.26987
3	2.0005 - 2.2005	1.5756 - 1.6106	0.26980 - 0.25438	0.24059 - 0.23529	0.26990 - 0.24542	0.24064 - 0.23540
4	2.2005 - 2.3006	1.6456 - 1.6675	0.25438 - 0.23464	0.22730 - 0.23031	0.24542 - 0.23475	0.22737 - 0.23040
5	2.3756 - 2.6407	1.6718 - 1.8907	0.22729 - 0.20448	0.22658 - 0.20042	0.22734 - 0.20452	0.22670 - 0.20053
6	2.7607 - 2.9527	1.9747 - 2.0419	0.19556 - 0.18278	0.19192- 0.18559	0.19563 - 0.18290	0.19200 - 0.18568
7	3.1688 - 3.1688	2.2688 - 2.3192	0.17037 - 0.17037	0.16703 - 0.16339	0.17043 - 0.17043	0.16711 - 0.16348
8	3.1688 - 3.3128	2.2688 - 2.3696	0.17037 - 0.16292	0.16703 - 0.15993	0.17043 - 0.16302	0.16711 - 0.16000
9	3.1688 - 3.3128	2.3696 - 2.4201	0.17037 - 0.16292	0.15993 - 0.15659	0.17043 - 0.16302	0.16000 - 0.15666
10	3.6297 - 3.8025	2.6923 - 2.7831	0.14867 - 0.14187	0.14075 - 0.13617	0.14879 - 0.14203	0.14082 - 0.13623

Table 6.18: Spice results vs 2D search results of CMOS NOR2 for rise time and fall time computation (0.35 μm, $V_{dd} = 3.3$ V)

Sl No.	**Spice input**		**Spice result**		**Nelder Mead algorithm**	
	w_P (μm)	w_N (μm)	$t_\mathbf{r}$(ps)	$t_\mathbf{f}$(ps)	$t_\mathbf{r}$ (ps)	$t_\mathbf{f}$ (ps)
1	1.8	0.9	10.400	10.299	10.420	10.340
2	1.9805	1.0345	9.276	9.289	9.3676	9.3005
3	2.0046	1.0458	9.005	8.982	8.9577	8.8935
4	2.2005	1.1678	8.345	8.820	8.5160	8.8455
5	2.4479	1.2587	7.6503	7.602	7.8063	7.7504
6	2.6257	1.3346	7.1023	7.101	7.2056	7.1542
7	3.1347	1.5709	6.2034	5.905	6.2450	6.2003
8	3.4223	1.6345	5.8328	5.8074	5.8547	5.8128
9	3.4356	1.7356	5.4039	5.3903	5.5103	5.4709
10	3.6	1.8	5.1054	5.2719	5.2090	5.1710

Table 6.19: Spice results vs NM results of CMOS secure circuit for rise time and fall time computation (180 nm, $V_{\rm dd} = 1.8$ V)

Sl No.	Spice input		Spice result		2D search algorithm	
	w_P (μm)	w_N (μm)	t_r(ps)	t_f(ps)	t_r(ps)	t_f(ps)
1	1.7817-1.8005	0.8958-0.9905	10.445 - 9.4565	10.3780 - 9.3887	10.457-9.4569	10.382-9.3892
2	1.9805-1.9805	0.9455-1.0356	9.9068 - 9.0451	9.8358 - 8.9801	9.9073-9.0458	9.8363-8.9810
3	1.8905-2.0706	1.0018-1.0581	9.3499 - 8.8528	9.2827 - 8.7889	9.3507-8.8533	9.2837-8.7899
4	1.9805-2.1381	1.0468-1.0749	8.9476 - 8.7137	8.8837 - 8.6508	8.9485-8.7142	8.8844-8.6518
5	2.1673-2.1606	1.0823-1.1887	8.6545 - 7.8799	8.5928 - 7.8237	8.6553-7.8808	8.5933-7.8243
6	2.3767-2.5927	1.2562-1.4264	7.4566 - 6.5666	7.4025 - 6.5668	7.4571-6.5673	7.4037-6.5203
7	2.6251-2.9816	1.4304-1.5236	6.5479 - 6.1475	6.5007 - 6.1035	6.5487-6.1481	6.5018-6.1041
8	3.1307-3.1113	1.5609-1.7120	6.0007 - 5.4721	5.9577 - 5.4328	6.0013-5.4728	5.9583-5.4336
9	3.4224-3.4224	1.6339-1.7894	5.7329 - 5.2338	5.6917 - 5.1965	5.7334-5.2348	5.6923-5.1973
10	3.2668-3.5779	1.7311-1.8283	5.4105 - 5.1227	5.3719 - 5.0858	5.4113-5.1234	5.3725-5.0867

Table 6.20: Spice results vs 2D search results of CMOS secure circuit for rise time and fall time computation (180 nm, $V_{dd} = 1.8$ V)

Chapter 7

Conclusion

In this chapter we summarize the contributions of this thesis.

7.1 Contributions

Modelling of CMOS circuits (CMOS inverter, NAND2, and NOR2) as a hybrid system at Level 2 has been done in the Matlab environment using Simulink/Stateflow modeling design tool. For checking the completeness of a model, reachability analysis scheme has been developed and successfully applied to confirm that the dead state is unreachable from the initial state in all cases. Different operating regions of the transistors are formulated using the differential equations that describes the circuit operation of CMOS circuits. The designed model is comparable with respect to the real circuit simulation results and execution time is fast.

The work reported has been extended to handle more complex combinational CMOS circuits modeled at higher level. Considering higher BSIM level equation, the current equation includes more device parameters for evaluating the behavior of the circuit accurately. Simulink Stateflow (hybrid system) modeling of transistor operation of precharge based logic circuits at BSIM3v3 level 49 has been done. Reachability analysis scheme has been developed and successfully applied to confirm that the dead state is unreachable from the initial state in all cases. The model designed using Stateflow simulink is comparable with respect to the real circuit simulation results and execution time is fast.

Given circuit performance requirements have been captured by formulating STL properties to capture desired properties (rise time, fall time and power). Parameter determination (transistor sizing) to achieve performance goals has been done using the Breach tool; Nelder mead (NM) algorithm and the presented two dimensional (2D) search algorithm has been used to

compare the parameters more efficiently. Using 2D search algorithm, the monotonicity properties of the responses of the rise and fall times and power estimates have been utilised. Using 2D search algorithm, it is possible to obtain a range of parameters with less computation time as compared to NM algorithm. The CMOS circuits are created using spice with optimised values of transistor width achieved through NM algorithm and 2D search algorithm to verify the stateflow model. The results of our technique have been compared with those of NM, RGA and DE algorithms. Only one parameter is obtained in those algorithms whereas using our technique a range of satisfiable parameters is obtained. Results obtained from NM and 2D search algorithms are comparable with the Spice results.

7.2 Future scope

Stateflow modeling as a hybrid system, other than digital circuits can be modeled. The dynamics of the DC motor can be modeled using stateflow modeling technique. The stateflow model of DC motor may consists of two superstates: powerOn and powerOff. If the motor is powered on, it can be in one of two substates: up or down, signifying the direction of movement.

The modelling technique descibed in the thesis can be utilised to model a non-MOSFET mathematical model. The Opamp inverting and noninverting circuit can be modeled using Matlab Simulink/stateflow designing tool. The monotonicity properties of the gain can be used to find the optimal value of feedback resistance and input resistance. Op-amp integrator is an operational amplifier circuit that performs the mathematical operation of integration, it can cause the output to respond to changes in the input voltage over time. The op-amp integrator produces an output voltage which is proportional to the integral of the input voltage. Similarly, Op-amp differentiator is an operational amplifier circuit that performs the mathematical operation of differentiation. It produces a output voltage which is directly proportional to the input voltage's rate-of-change with respect to time. By applying different signals such as a square-wave, triangular or sine-wave to the input of a differentiator or integrator amplifier circuit the resultant output signal will be changed and is dependant upon the Resistor or Capacitor combination. Thus, the algorithm described can be used to find the optimal value of resistor and capacitor.

The algorithm described in the thesis for transistor sizing contains two step process. Although the algorithm is faster than the NM algorithm, can be extended to find other parameters such as load capacitance and supply voltage.

Appendix A

Physical and Materials Constants

Boltzmann's constant	k	1.38×10^{-23}	J/K
Electron charge	q	1.6×10^{-19}	C
Free Space Permittivity	ϵ_o	8.85×10^{-14}	F/cm
Dielectric constant of silicon (Si)	ϵ_{si}	$11.7 \times \epsilon_o$	F/cm
Dielectric constant of silicon dioxide (SiO_2)	ϵ_{ox}	$3.97 \times \epsilon_o$	F/cm

Appendix B

SPICE Model Parameters of MOSFETS

Name	**Model Parameters**	**Units**	**Defaults**
LEVEL	Model type (1, 2, or 3)		1
L	Channel length	m	DEFL
W	Channel width	m	DEFW
V_{t0}	Zero-bias threshold voltage	V	0
k_p	Transconductance	A/V^2	$2.00e-05$
gamma	Bulk threshold parameter	$V^{1/2}$	0
ϕ_f	Surface potential	V	0.6
Lambda	Channel-length modulation (LEVEL = 1or 2)	V^{-1}	0
JS	Bulk p-n saturation/current area	A/m^2	0
C_j	Bulk p-n zero-bias bottom capacitance/length	F/m^2	0
C_{jsw}	Bulk p-n zero-bias perimeter capacitance/length	F/m	0
C_{gso}	Gate-source overlap capacitance/channel width	F/m	0
C_{gdo}	Gate-drain overlap capacitance/channel width	F/m	0
C_{gbo}	Gate-bulk overlap capacitance/channel width	F/m	0
NSUB	Substate doping density	cm^{-3}	0
NSS	Surface-state density	cm^{-2}	0
NFS	Fast surface-state density	cm^{-2}	0
t_{ox}	Oxide thickness	m	∞

TPG	Gate material type: + 1 =opposite of substrate, - 1 =same as substrate, 0 =aluminum		+1
xj	Metallurgical junction depth	m	0
UCRIT	Mobility degradation critical field (LEVEL = 2)	V/cm	1.00e+04
UEXP	Mobility degradation exponent (LEVEL = 2)		0
UTRA	(Not Used) mobility degradation transverse field coefficient		
VMAX	Maximum drift velocity	m/s	0
NEFF	Channel charge coefficient (LEVEL = 2)		1

Appendix C

SPICE Model Parameters of MOSFETS - Level 49

Name	Model Parameters	Units	Defaults
t_{ox}	gate oxide thickness	m	150e-10
xj	junction depth	m	0.15e-6
V_{t0}	threshold voltage of long channel device at $V_{bs} = 0$ and small V_{ds} (typically 0.7 for n- channel, - 0.7 for p-channel)	V	0.7
NSUB	substrate doping concentration	cm-3	6.0e16
nchannel	peak doping concentration near interface	cm-3	1.7e17
nlx	lateral nonuniform doping along channel	m	1.74e-7
k_1	first-order body effect coefficient	$V^{1/2}$	0.50
k_2	second-order body effect coefficient	-	-0.0186
k_3	narrow width effect coefficient	-	80.0
k_{3b}	body width coefficient of narrow width effect	V^{-1}	0
$w0$	narrow width effect coefficient	m	2.5e-6
dvt0	short channel effect coefficient 0, for Vth	-	2.2
dvt1	short channel effect coefficient 1, for Vth	-	0.53
dvt2	short channel effect coefficient 2, for Vth	V^{-1}	-0.032
V_{bm}	maximum substrate bias, for V th calculation	V	-3.0

μ_0	low field mobility at T = TREF = TNOM	$cm^2/V/s$	670 nmos 250 pmos
μ_a	first-order mobility degradation coefficient	m/V	2.25e-9
μ_b	second-order mobility degradation coefficient	m^2/V^2	5.87e-19
μ_c	body bias sensitivity coefficient of mobility -4.65e-11 for MOBMOD=1,2 or, -0.0465 for MOBMOD = 3	V^{-1}	-4.65e-11 or -0.0465
a0	bulk charge effect coefficient for channel length	-	1.0
b0	bulk charge effect coefficient for channel width	m	0.0
b1	bulk charge effect width offset	m	0.0
keta	body-bias coefficient of bulk charge effect	V^{-1}	-0.047
vsat	saturation velocity of carrier at T = TREF = TNOM	m/s	8e4
a1	first nonsaturation factor	V^{-1}	0
a2	second nonsaturation factor	-	1.0
R_{DSW}	parasitic source drain resistance per unit width	$\Omega\ \mu$m	0.0
pclm	coefficient of channel length modulation values < 0 will result in an error message and program exit	-	1.3
pdibl1	DIBL (Drain Induced Barrier Lowering) effect coefficient 1	-	0.39
pdibl2	DIBL effect coefficient 2	-	0.0086
drout	length dependence coefficient of the DIBL correction parameter in R out	-	0.56
pavg	gate dependence of Early voltage	-	0
γ_1	body effect coefficient near the surface	$V^{1/2}$	-
γ_2	body effect coefficient in the bulk	$V^{1/2}$	-
V_{bx}	V_{bx} at which the depletion region width equals X_t	V	-
X_t	doping depth	m	1.55e-7
V_{bi}	drain and source junction built-in potential	V	-
ϕ_s	bulk junction contact potential	V	1.0

Bibliography

[1] A. A. Hamoui and N. C. Rumin, "An analytical model for current, delay, and power analysis of submicron CMOS logic circuits," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 47, pp. 999 –1007, 2000.

[2] J. R. Brews, *Physics of the MOS transistor', in Silicon Integrated Circuits (D. Kahng, Ed.).* Applied Solid-state Science Series, Supplement 2A, Academic Press, New York, 1981.

[3] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor.*

[4] H. C. de Graaff and F. M. Klaassen, *Compact Transistor Modelling for Circuit Design.* Springer-Verlag Wien, New York, 1990.

[5] D. A. Divekar, *FET Modeling for Circuit Simulation.* Kluwer Academic Publisher, Boston, 1988.

[6] P. Antognetti and G. Massobrio, *Semiconductor Device Modeling with SPICE.* McGraw-Hill Book Company, New York,, 1988.

[7] L. Bisdounis, O. Koufopavlou, C. Goutis, and S. Nikolaidis, "Switching response modeling of the CMOS inverter for sub-micron devices.," pp. 729–735, Jan 1998.

[8] J.-M. Shyu, A. S-Vincentelli, and J. P. Fishburn, "Optimization-based transistor sizing," *IEEE Journal of Solid-State Circuits*, vol. 23, April 1988.

[9] J. M. Rabaey, *Digital Integrated Circuits A Design Perspective.* 1995.

[10] *Stateflow and Stateflow Coder User's Guide.* The MathWorks, march 2009.

[11] Y. Yang, Y. Jiang, M. Gu, and J. Sun, "Verifying simulink/stateflow model: timed automata approach," in *Proc. of 31st IEEE/ACM International Conference on Automated Software Engineering, ASE*, 2016.

[12] A. Agrawal, G. Simon, and G. Karsai, "Semantic translation of simulink/stateflow models to hybrid automata using graph transformations," in *Electronic Notes in Theoretical Computer Science*, vol. 109, pp. 43–56, December 2004.

[13] H. Bourbouh, P. Garoche, C. Garion, A. Gurfinkel, T. Kahsai, and X. Thirioux, "Automated analysis of stateflow models," *21st International Conference on Logic for Programming, Artificial Intelligence and Reasoning*, vol. 46, pp. 144–161, 2017.

[14] A. Donzé, T. Ferrére, and O. Maler, "Efficient robust monitoring for STL," *International Conference on Computer Aided Verification*, pp. 264–279, 2013.

[15] A. Donzé, "Breach, a toolbox for verification and parameter synthesis of hybrid systems," *International Conference on Computer Aided Verification*, pp. 167–170, 2010.

[16] A. Girard and G. J. Pappas, "Verification using simulation," *International Workshop on Hybrid Systems: Computation and Control*, pp. 272–286, 2006.

[17] A. Donzé, O. Maler, E. Bartocci, D. Nickovic, R. Grosu, and S. Smolka, "On temporal logic and signal processing," *International Symposium on Automated Technology for Verification and Analysis*, pp. 92–106, 2012.

[18] J. Haase and M. Dietrich, *Process Variations and Probabilistic Integrated Circuit Design*. Springer-Verlag New York, 1 ed., 2012.

[19] A. I. Kayssi, K. A. Sakallah, and T. M. Burks, "Analytical transient response of CMOS inverters," *IEEE Trans. Circuits and Systems-I*, vol. 39, pp. 42–45, January 1992.

[20] K. Doganis and D. L. Scharfetter, "General optimization and extraction of IC device model parameters," *IEEE Transactions on Electron devices*, vol. 30, pp. 1219–1228, 1983.

[21] P. R. Karlsson and K. O. Jeppson, "A direct extraction algorithm for a submicron MOS transistor model," in *Proc. of the 1993 International Conference on Microelectronic Test Structures*, p. 157âĂŞ162, 1993.

[22] P. Chaourani, I. Messaris, N. Fasarakis, M. Ntogramatzi, S. Goudos, and S. Nikolaidis, "An analytical model for the CMOS inverter," *24th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, 2014.

[23] E. Consoli, G. Giustolisi, and G. Palumbo, "An accurate ultra-compact I-V model for nanometer mos transistors with applications on digital circuits," *IEEE Transactions Circuits Systems*, vol. 59, Jan. 2012.

[24] S. M. S. S. Dutta and S. Lusky, "A comprehensive delay model for cmos inverters," *IEEE J. Solid-State Circuits*, vol. 30, pp. 864–871, Aug 1995.

[25] B. J. Sheu, D. L. Scharfetter, P.-K. Ko, and M.-C. Jeng, "Bsim: Berkeley short-channel IGFET model for MOS transistors," *IEEE Journal of Solid-state Circuits*, vol. 22, pp. 558–566, 1987.

[26] R. A. Rutenbar, G. G. E. Gielen, and J. Roychowdhury, "Hierarchical modeling, optimization, and synthesis for system-level analog and rf designs," in *Proceedings of the IEEE*, vol. 95, pp. 640–669, 2007.

[27] A. Klös and A. Kostka, "Predictmos - a predictive compact model of small-geometry MOSFETs for circuit simulation and device scaling calculations," *Solid-State Electronics*, vol. 44, no. 7, pp. 1145–1156, 2000.

[28] Y. W.Zhao, "Predictive technology model for nano-cmos design exploration," in *Proc. ACM Journal in Emerging Technologies in Computing Systems*, vol. 3, pp. 2–17, April 2007.

[29] J. Mukhopadhyay and S. Pandit, "Design of a nano-scale CMOS inverter with symmetric switching characteristics using particle swarm optimization algorithm," *IEMCON*, 2012.

[30] T.McConaghy and G.Gielen, "Automation in mixed-signal design: Challenges and solutions in the wake of nano era," *ICCAD*, pp. 461–463, 2006.

[31] L. Bisdounis, S. Nikolaidis, and O. Koufopavlou, "Analytical transient response and propagation delay evaluation of the CMOS inverter for short-channel devices," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 302–306, 1998.

[32] Z.-H. Liu, C. Hu, J.-H. Huang, T.-Y. Chan, M.-C. Jeng, P. K. KO, and Y. C. Cheng, "Threshold voltage model for deep-submicrometer MOSFET's," *IEEE Transactions on electron devices*, vol. 40, no. 1, 1993.

[33] H. S. Lee, "An analysis of the threshold voltage for short-channel IGFET's," *Solid-state Electron*, vol. 16, pp. 1407–1417, 1973.

[34] T. Toyabe and S. Asai, "Analytical models of threshold voltage and breakdown voltage of short-channel MOSFET's derived from two dimensional analysis," *IEEE Journal of Solid-State Circuits*, vol. 14, no. 4, pp. 453 – 461, 1979.

[35] D. R. Poole and D. L. Kwong, "Two-dimensional analysis modeling of threshold voltage of short-channel MOSFET's," *IEEE Electron Device Letters(EDL)*, vol. 5, no. 11, pp. 443 – 446, 1984.

[36] R.Krambeck, C. Lee, and H. Law, "High-speed compact circuit with cmos," *IEEE Journal of Solid- state Circuits*, vol. 17, pp. 614–619, 1982.

[37] V.Oklobdzija and R.Montoya, "Design-performance trade off in cmos-domino logic," *IEEE journal of Solid-state Circuit*, vol. 21.

[38] E. Sicard and S. D. Bendhia, *Basics of CMOS Cell Design.* Mc-Graw Hill, USA, 2007.

[39] A. E. Ruehli, P. K. Wolff, and G. Goertzel, "Analytical power timing optimization technique for digital system," in *in Proceedings of the 14th Design Automation Conference*, pp. 142–146, June 1977.

[40] W. T. Nye, A. L. Sangiovanni-Vincenteli, J. P. Spoto, and A. L. Tits, "Delight-spice: an optimization-based system for the design of ic," in *in Proceedings of the IEEE Custom Integrated Circuits Conference*, p. 233âĂŞ238, May 1983.

[41] S. K. Karandikar and S. S. Sapatnekar, "Fast comparisons of circuit implementations," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 13, no. 12, pp. 1329–1339, 2005.

[42] S. Dutta, S. Nag, and K. Roy, "ASAP: a transistor sizing tool for speed, area, and power optimization of static CMOS circuits," in *Proceedings of IEEE International Symposium on Circuits and Systems - ISCAS '94*, vol. 1, pp. 61–64 vol.1, May 1994.

[43] N. Hedenstiema and K. Jeppson, "CMOS circuit speed and buffer optimization," *IEEE Trans. Computer-Aided Design*, vol. 6, pp. 270–281, March 1987.

[44] K. O. Jeppson, "Modeling the influence of the transistor gain ratio and the input-to-output coupling capacitance on the CMOS inverter delay," *IEEE J. Solid-state Circuits*, vol. 29, pp. 646–654, June 1994.

[45] S. Vemuru and A. Thorbjornsen, "A model for delay evaluation of a CMOS inverter," in *In Proc. of lSCAS*, vol. 1, pp. 89–92, May 1990.

[46] H. J. M. Veendrick, "Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits," *IEEE Journal of Solid-State Circuits*, vol. 19, pp. 468–473, Aug. 1984.

[47] H. Shichman and D. A. Hodges, "Modeling and simulation of insulated gate field-effect transistor switching circuits," *IEEE Journal of Solid-State Circuits*, vol. 3, pp. 285–289, Sept. 1968.

[48] L. Bisdounis, S. Nikolaidis, O. Koufopavlou, and C. E. Goutis, "Modeling the CMOS short-circuit power dissipation," in *Proc. IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 469–472, May 1996.

[49] A. Chatzigeorgiou and S. Nikolaidis, "Efficient output waveform evaluation of a cmos inverter based on short-circuit current prediction," *International Journal of Circuit Theory and Applications*, vol. 30, Sept 2002.

[50] M. Borah, R. M. Owens, and M. J. Irwin, "Transistor sizing for minimizing power consumption of CMOS circuits under delay constraint," in *Proc. of International symposium on Low Power Design*, pp. 167–172, 1995.

[51] P. C. Anantha, S. Samuel, and W. B. Robert, "Low-power CMOS digital design," *IEEE Journal of Solid-State Circuits*, vol. 27, April 1992.

[52] W. Liu, *MOSFET Models for SPICE Simulation Including BSIM3v3 and BSIM4*. Wiley Interscience, 2001.

[53] Y. H. Hu and S. Pan, "SaPOSM: an optimization method applied to parameter extraction of MOSFET models," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 12, no. 10, pp. 1481–1487, 1993.

[54] W. Liu, X. Jin, X. Xi, J. Chen, M. Jeng, Z. Liu, Y. Cheng, K. Chen, M. Chan, K. Hui, J. Huang, R. Tu, K. P. Ko, and C. Hu, *BSIM3V3.3 User's Manual. Department of Electrical Engineering and Computer Sciences*. University of California, Berkeley, 2005.

[55] T. Sakurai, B. Lin, and A. R. Newton, "Fast simulated diffusion: an optimization algorithm for multiminimum problems and its application to MOSFET model parameter extraction," *IEEE Transactions on*

Computer-Aided Design of Integrated Circuits and Systems, vol. 11, no. 2, pp. 228–234, 1992.

[56] T. Sakurai and R. Newton, "Alpha-power law MOSFET model and its application to CMOS inverter delay and other formulas," *IEEE Journal of Sold State Circuits*, vol. 25, pp. 584–594, 1990.

[57] T. Sakurai and R. Newton, "A simple MOSFET model for circuit analysis," *IEEE Trans Electron Device*, vol. 38, pp. 887–894, 1991.

[58] A. Nunez and R. Vemuri, "An analog performance estimator for improving the effectiveness of cmos analog systems circuit synthesis,"

[59] J. Kennedy and R. C. Eberhart, "Particle swarm optimization," in *Proc. of IEEE International Conference on Neural Networks*, 1995.

[60] B. PrasadDe, R. Kar, D. Mandal, and S. P. Ghoshal, "Optimal CMOS inverter design using differential evolution algorithm," *Journal of Electrical Systems and Information Technology*, vol. 2, pp. 219–241, September 2015.

[61] R. A. Vural, O. Der, and T. Yildirim, "Investigation of particle swarm optimization for switching characterization of inverter design," *Expert Systems with Applicatopns*, vol. 38, no. 5, 2011.

[62] R. A. Vural and T. Y. O. Der, "Particle swarm optimization based inverter design considering transient performance," *Digital Signal Processing*, vol. 20, no. 4, pp. 1215–1220, 2010.

[63] W. E. Hart, N. Krasnogor, and J. E. Smith, *Recent Advances in Memetic Algorithms*. Springer, Berlin, Heidelberg, New York, 2005.

[64] D. Harel, "Statecharts: A visual formalism for complex systems," in *Science of Computer Programming*, vol. 8, pp. 231–274, 1987.

[65] C. Chen, J. Sun, Y. Liu, J. S. Dong, and M. Zheng, "Formal modeling and validation of stateflow diagrams," *International Journal on Software Tools for Technology Transfer*, vol. 14, no. 6, pp. 653 – 671.

[66] A. Vladimirescu and S. Liu, "The simulation of MOS integrated circuits using SPICE2," Tech. Rep. UCB/ERL M80/7, EECS Department, University of California, Berkeley, 1980.

[67] A. S. Grove, *Physics and Technology of Semicondudor Devices*. Wiley, New-York, 1967.

[68] R. S. . Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*. Wiley, New-York, 1977.

[69] D. Frohman-Bentchkowsky, "On the effect of mobility variation on MOS device characteristics," in *Proceedings of the IEEE*, vol. 56, pp. 217– 218, February 1968.

[70] N. Arora, *MOSFET Modelling for VLSI simulation Theory and Practice*. World Scientific Publishing Co. Re. Ltd, 2007.

[71] H. Guéguen, M. A. Lefebvre, J. Zaytoon, and O. Nasri, "Safety verification and reachability analysis for hybrid systems," *Annual Reviews in Control*, vol. 33, 2009.

[72] M. Avci, M. Y. Babac, and T. Yildirim, "Neural network based mosfet channel length and width decision method for analogue integrated circuits," *International Journal of Electronics*, vol. 92, no. 5, pp. 281–293, 2005.

[73] Avant, *Star-Hspice Manual*. July 1998.

[74] P. De, C. Mandal, and U. Prampalli, "Path-balanced logic design to realize block ciphers resistant to power and timing attacks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 5, pp. 1080–1092, 2019.

[75] K. Tiri and I. Verbauwhede, "A logic level design methodology for a secure DPA resistant ASIC or FPGA implementation," in *Proceedings Design, Automation and Test in Europe Conference and Exhibition*, vol. 1, pp. 246–251, 2004.

[76] L. N. Ramakrishnan, M. Chakkaravarthy, A. S. Manchanda, M. Borowczak, and R. Vemuri, "SDMLp: On the use of complementary pass transistor logic for design of DPA resistant circuits," in *2012 IEEE International Symposium on Hardware-Oriented Security and Trust*, pp. 31–36, 2012.

[77] P. De, K. Banerjee, C. Mandal, and D. Mukhopadhyay, "Circuits and synthesis mechanism for hardware design to counter power analysis attacks," in *2014 17th Euromicro Conference on Digital System Design*, pp. 520–527, 2014.

[78] O. Maler and D. Nickovic, "Monitoring temporal properties of continuous signals," *FORMATS/FTRTFT*, pp. 152–166, 2004.

[79] O. Maler, D. Nickovic, and A. Pnueli, "From MITL to timed automata," *FORMATS*, pp. 274–289, 2006.

[80] H. Roehm, J. Oehlerking, T. Heinz, and M. Althoff, "STL model checking of continuous and hybrid systems," *International Symposium on Automated Technology for Verification and Analysis*, pp. 412–427, 2016.

[81] J. A. Nelder and R. Mead, "A simplex method for function minimization," *The computer Journal*, vol. 7, pp. 308–313, 1965.

[82] H. Lin, "Hybridizing differential evolution and Nelder-Mead simplex algorithm for global optimization," *12th International Conference on Computational Intelligence and Security (CIS)*, 2016.

[83] *AIM-Spice Reference Manual*. 2014.

[84] B. Sheu, D. Scharfetter, Chenming Hu, and D. Pederson, "A compact IGFET charge model," *IEEE Transactions on Circuits and Systems*, vol. 31, no. 8, pp. 745–748, 1984.

[85] S. S. . Chung, "A charge-based capacitance model of short-channel MOSFETs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 8, no. 1, pp. 1–7, 1989.

[86] B. Sheu, D. Scharfetter, and P. Ko, "SPICE2 implementation of bsim," Tech. Rep. UCB/ERL M85/42, EECS Department, University of California, Berkeley, May 1985.

[87] J. E. Meyer, "MOS models and circuit simulation," *RCA Rev.*, vol. 32, pp. 42–63, 1971.

[88] D. E. Ward and R. W. Dutton, "A charge-oriented model for MOS transistor capacitances," *IEEE Journal of Solid-State Circuits*, vol. 13, no. 5, pp. 703–708, 1978.

[89] A.S.Grove and D.J.Fitzgerald, "Surface effects on p-n junctions: Characteristics of surface space-charge regions under non-equilibrium conditions," *Solid-State Electronics*, vol. 9, pp. 783–806, 1966.

[90] M. S. Mock, "A two-dimensional mathematical model of the insulated-gate field-effect transistor," *Solid-state Electron.*, vol. 16, pp. 601–609, 1973.

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