Signaling Design Automation Tool for EIs (SigDATE)

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Abstract

Commissioning any new signalling work or alterations in the existing signalling interlocking of the station is a tedious task. The process involves various technical documents such as signal interlocking plan (SIP), route control chart (RCC), application logic circuits of EIs, etc. Designing and checking these documents require expertise in signalling principles and rules. Usually, design and drawing cells of the zonal railways deal with checking and approving these design documents, which is time-consuming as it is done manually. A need has been felt to automate this entire process to save time and expedite the commissioning of EI works.

Keywords: SigDATE, GUI, EI, SIP, RCC

1. Introduction

Signalling Design Automation Tool for EIs (SigDATE) has been developed indigenously by the Research Design and Standards Organisation, Lucknow and the Indian Institute of Technology, Kharagpur. With the help of this tool, the Route Control Chart (RCC) for commissioning of Electronic Interlocking (EI) systems can be automatically generated by capturing the Signal Interlocking Plan (SIP) of station yards. This tool provides a graphical user interface (GUI) for capturing the signal interlocking plan in electronic form. It uses internal data structure to store the geometric data of the yard for further processing. SIP contains details like location and type of signals (main signals like home signals, starter signals, advance starter signals etc., subsidiary signals like independent shunt signals, dependant shunt signals, calling on signals etc.), track detection system (track circuits, axle counters etc.), points (double ended, single-ended etc.), signal overlaps, block overlap, block working etc.

2. GUI

GUI of SigDATE consists of a palette of yard elements, such as track circuits, points, signals, level crossings etc., on the right side (Figure 1). It has inbuilt option of various types of signals

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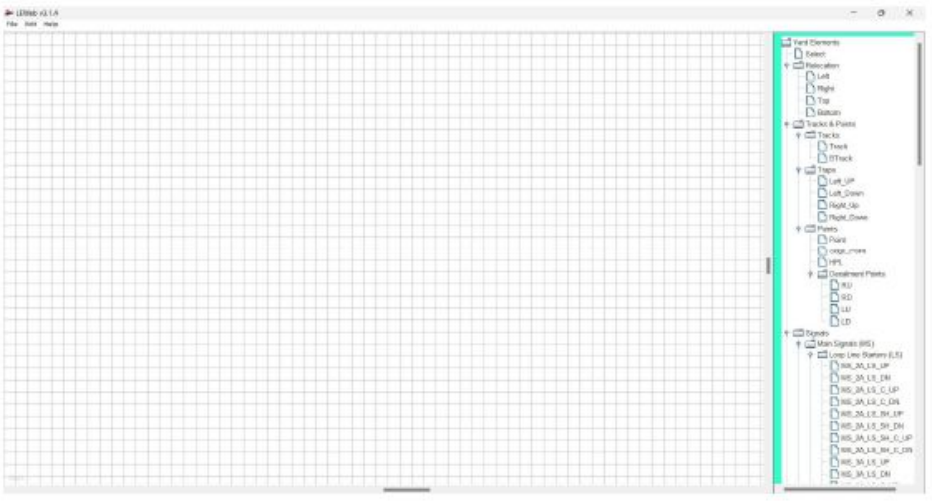

Fig.1: SigDATE GUI

(like 2/3/4 aspect main signals, dependent and independent shunt signals, calling on signals, automatic signals, IB signals, gate signals, distant signals etc.), points (double ended points, trap points etc.), track circuits, stop boards, warning boards etc. A few options available in SigDATE for selecting signals, points etc., are given in figure 2 and 3.

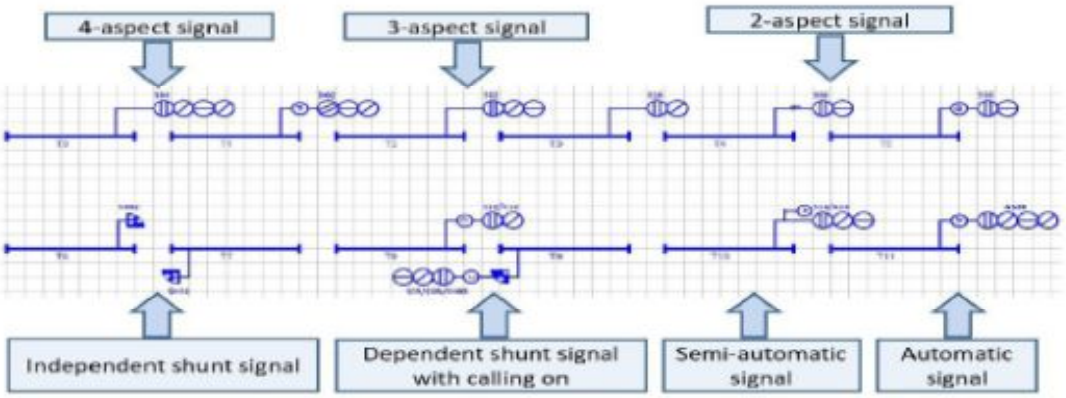

Fig. 2: Different combination of signals

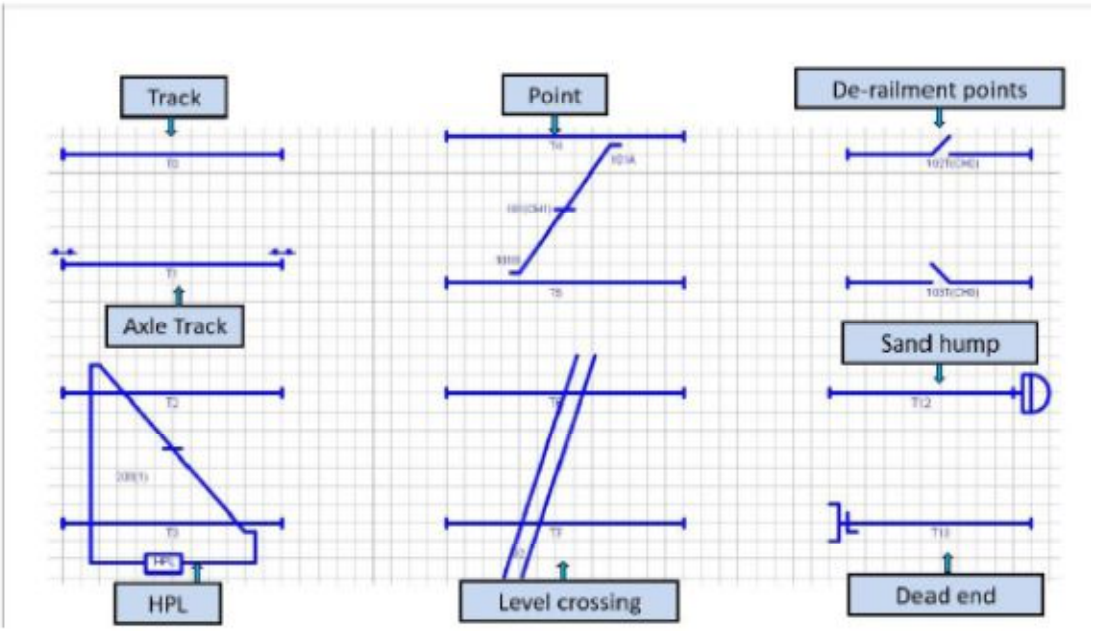

Fig. 3: Different types of points

Various signals, points, etc., can be selected from the SigDATE graphical user interface and placed on the drawing canvas to prepare the signal interlocking plan in electronic form. A pictorial representation of captured signal interlocking plan is given below as figure 4.

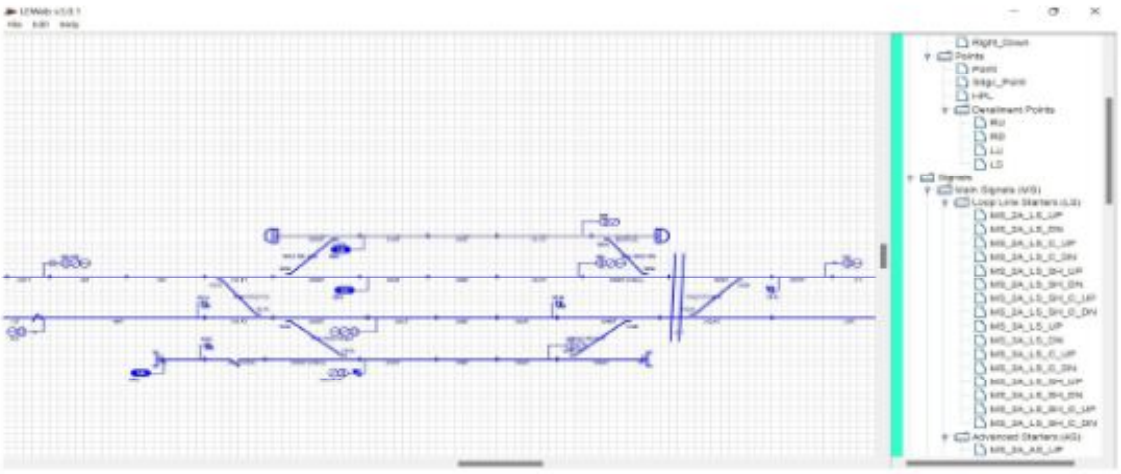

Fig. 4: Sample yard captured in SigDATE

3. Generation of RCC

SIP is stored in a machine-readable XML format for reuse. It usually takes only 1-2 hours to design a SIP with the use of SigDATE for typical four-line stations, which is considerably less compared to manual design time. Once the SIP is electronically captured, this tool can automatically generate a route control chart (RCC) which includes details of the necessary condition of points, track circuits, signals, etc., overlap and isolation for each route of signal interlocking. It usually takes only a few seconds to generate RCC from the SIP of a typical four-line station using SigDATE, whereas it requires a few days to manually design RCC from a given SIP. The captured SIP and generated RCC are further formally validated [1] to ensure the yard and the corresponding interlocking plan satisfy the basic operational and safety principles of Indian Railways. A pictorial representation of generated route control chart is shown below in figure 5.

Fig. 5: Sample yard captured in SigDATE

4. Conclusion

SigDATE is the indigenously developed tool for signalling design that drastically reduces the time required for preparing the route control chart will be drastically reduced. This tool will be handy for the officials who deal with design and drawing matters of the signalling department of all the zonal railways. This will help expedite the commissioning of new infrastructure works over Indian Railways. On 23rd August 2022, the automation tool, SigDATE was officially inaugurated by the Chairman & CEO of the Railway Board. Initially, this tool is being used to design SIP and RCC for stations having routes up to 100. Further generation of logic circuits from captured SIP and generated RCC is under development in the SigDATE automation tool.

5. References

[1] A. Das, M. K. Gangwar, D. Ghosh, C. Mandal, A. Sengupta, M. M. Waris, Automatic generation of route control chart from validated signal interlocking plan, IEEE Transactions on Intelligent Transportation Systems 22 (2021) 6516–6525. doi:10.1109/TITS.2020.2993794.

Shri Amit Misra, IRSSE, BE in Electronics Engineering from Motilal Nehru National Institute of technology, Prayagraj, Uttar Pradesh. Currently he's working as Executive Director Signal in RDSO, Lucknow. Prior to this, he has worked in maintenance and construction organisations of North central railways in Prayagraj and Jhansi divisions.

Shri Professor Chittaranjan Mandal, SMIEEE, worked in many areas such as wayside railway signal design, networking, formal verification, secure circuit design and computational biology. He has also been associated with national level programmes such as development of virtual laboratories which have served students well during the Covid period and SMILE (Software for Managing Institutes of Learning and Education) ERP which have already been adopted by some NITs (Bhopal, Warangal) and also IIEST Shibpur and are being adopted by other institutes also. His work on signalling has culminated in the development of the SigDATE tool. Presently with the Dept. of Computer Science and Engineering, IIT Kharagpur, joined in 1999 after serving as Reader with Jadavpur University. He received a Royal Society Fellowship for conducting collaborative work with Kingston University where he was also an Industrial Fellow. He has handled sponsored projects from several Indian government bodies and multinational companies. He is a reviewer for reputed journals, supervised several PhD students and has several publications some of which have attracted best paper awards and significant citations.

Shri Shankhadip Mallick Senior research scholar at the Dept. of Computer Science, IIT Kharagpur. He worked at IIT Kanpur and completed two national-level projects in the area of formal verification and closely associated with the ongoing railway signalling projects at IIT Kharagpur. He also carried out some major development activities in the SMILE ERP, which is being adapted in different technical institutes of national importance. Currently, he looks after all the development and maintenance activities related to the SigDATE tool.