High Level Synthesis of Linear Analog Systems

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Outline

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- Architecture Synthesis
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Motivation

- Bottom-up design for analog circuits
  - Low productivity
  - Reduced possibility of system-level optimization
  - Inadequate system verification
- Top-down design is more efficient and less costly than bottom-up design.
- For high performance analog system design, system level synthesis and optimization must precede circuit level details.

Related Work

- ARCHGEN and ARCHSIM (*B.A.A.Antao, 1995*)
  - State Space representation of the systems
  - Synthesis of Intermediate Architecture
  - Behavioral Simulation for Verification
- Exploration based Synthesis guided by the Signal flow Graph of a system starting from an HDL description. (Doboli & Vemuri, 2003)
- Two-layer Library based approach to synthesis of analog systems from VHDL-AMS specs (Doboli & Vemuri, 2004)

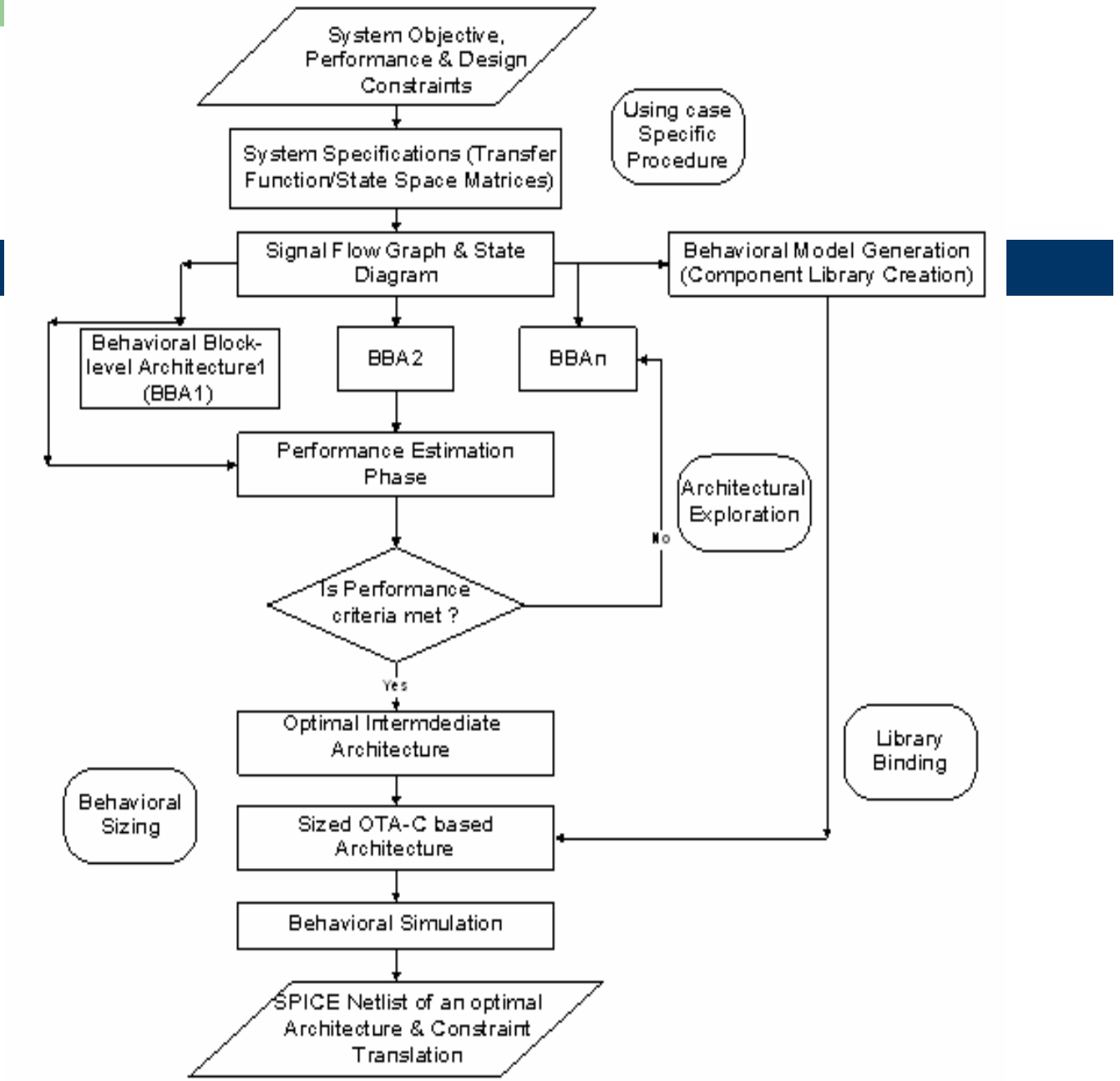
Limitations of Previous Work

- Heuristics based Architecture Synthesis Procedure
- Lack of Optimal Topology Synthesis
- Lack of Hierarchical Sizing of Circuits
- System dependent

High Level Synthesis Methodology

- Analog and Mixed Signal High Level Synthesis consists of four main tasks
  - System Specification
  - Architecture Synthesis (System netlist Generation)
  - Performance Model Generation
  - Constraint Transformation
- Input: Desired specifications
- Output: Optimal sized architecture and constraints which are to be passed to the next level of design hierarchy.

Proposed Methodology



State Space Model and SFG

$$s\mathbf{x}(s) = \mathbf{A}\mathbf{x}(s) + \mathbf{B}\mathbf{u}(s)$$

$$y(s) = \mathbf{C}\mathbf{x}(s) + Du(s)$$

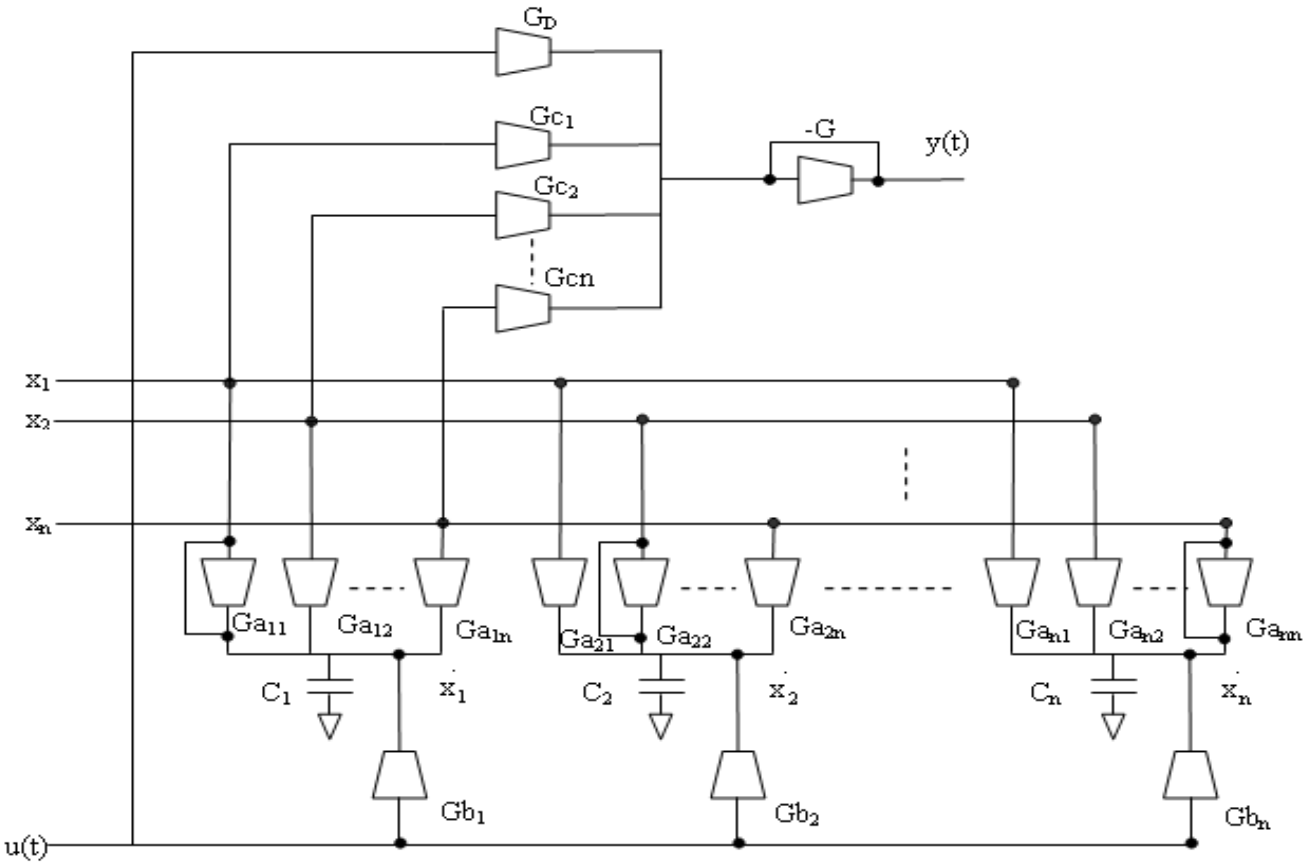
where **A**,**B**,**C**,D are real state space matrices.

- Signal Flow Graph (SFG) represents the above set of linear equations
- State space models are not unique. All models are behaviorally equivalent but differs in performance measure.

Architecture Synthesis

- In the first step behavioral block level architectures are generated from the SFG.
- BBAs are behavioral structures composed of implementation style independent functional units like adders, scalars, integrators.
- In the second step, the behavioral blocks are replaced with appropriate OTA based circuits.
- Gm values determined from the state space matrix elements.

Generic OTA Structure



Sensitivity Optimization

- Sensitivity to circuit parameter variations is a vital performance metric, providing an indication on the manufacturability of a particular design.
- Sensitivity analysis provides tolerance levels for the sizes and constraints for the synthesized architectures.
- L2 norm measure of the sensitivity matrix is a realistic choice of the measure.

Cost Function

$$S_{L2}(\mathbf{P}) = tr\left[\frac{1}{2\pi}\int_0^{2\pi} \mathbf{P}\mathbf{N}\left(e^{j\omega}\right)\mathbf{P}^{-1}\mathbf{N}^{T}\left(e^{-j\omega}\right)d\omega\right] + tr\left(\mathbf{P}\mathbf{W}\right) + tr\left(\mathbf{P}^{-1}\mathbf{K}\right)$$

W and **K** are the observability Gramian and controllability Gramian matrices respectively. **N** is another Gramian matrix, all related to state space matrices **(A,B,C**,D). **P=TT'** where **T** is the similarity transformation matrix.

- Thus the L2 sensitivity value is architecture dependent.

Optimization Strategy

- Hybrid Approach using statistical global search (SA) and deterministic local search (Gradient based) procedures.
- While exploring the architecture space, check that the matrix **P** is positive symmetric and the architectural solution points are stable so that Gramians are defined.

Experiment: Low Pass Filter Synthesis

- **Desired Specification**: Passband Gain between 0 dB and -2 dB; Stopband Gain at least -20 dB; Cut off frequency 10 Hz. Sensitivity < 8%.
- From Matlab toolbox simulation, order = 4, assuming Butterworth specifications. Transfer function and initial state space model determined.
- Optimal state space determined using the optimization strategy.
- From the optimal state space model and the SFG, BBA and Gm-C structure determined. Gm sizes calculated from the model.
- SPICE simulation and Monte Carlo analysis of the resultant architecture.

Synthesis Results

Parameters	Specifications	Synthesis Results
Passband Gain	0 dB and -2 dB	-0.2 dB
Stopband Gain	At least -20 dB	-35 dB
Cut off Frequency	10 Hz	15 Hz
Sensitivity	< 8 %	6.64 %

Simulation Plots

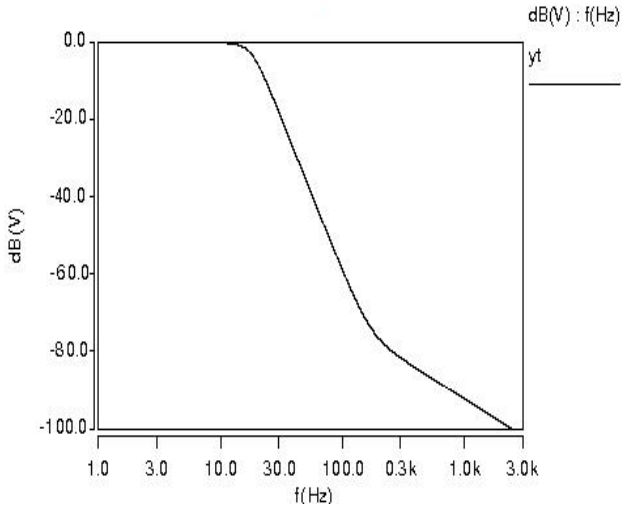
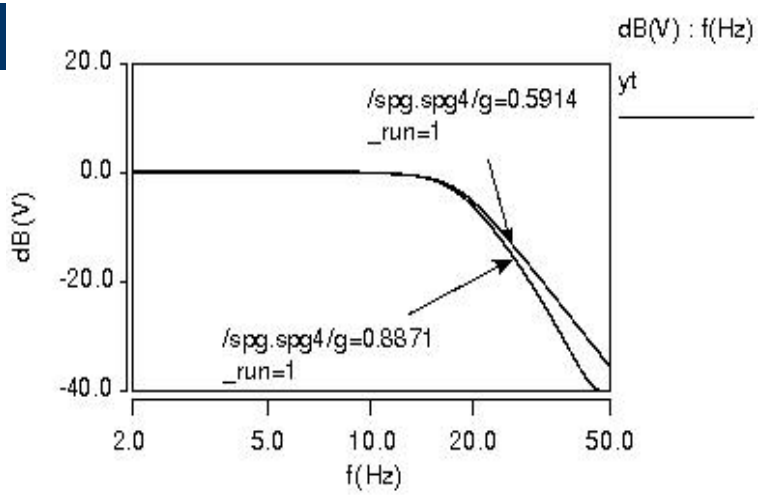


Figure 1: Bode Plot



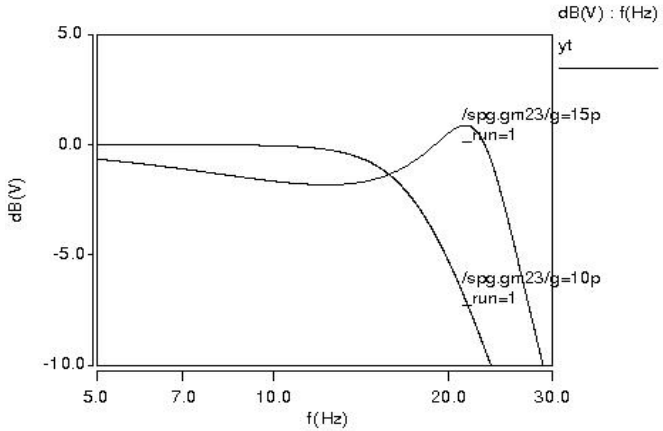


Figure 2(a),(b): Monte Carlo analysis of controllability and optimized architecture.

Conclusion

- Formal Approach to High Level Synthesis of analog systems
- Reduces the labour of circuit designers by providing sized optimal architecture with proper tolerances and other constraints.
- L2 sensitivity of the synthesized architecture is minimized.
- Allows hierarchical synthesis of robust analog systems in short time without requiring detailed analog knowledge.