

Early Routability Assessment in VLSI Floorplans: A Generalized Routing Model

BAPI KAR, Indian Institute of Technology Kharagpur SUSMITA SUR-KOLAY, Indian Statistical Institute Kolkata CHITTARANJAN MANDAL, Indian Institute of Technology Kharagpur

Multiple design iterations are inevitable in nanometer Integrated Circuit (IC) design flow until desired printability and performance metrics are achieved. This starts with placement optimization aimed at improving routability, wirelength, congestion and timing in the design. Contrarily, no such practice exists on a floorplanned layout, during the early stage of the design flow. Recently, STAIRoute [19] aimed to address that by identifying the shortest routing path of a net through a set of routing regions in the floorplan in multiple metal layers. Since the blocks in hierarchical ASIC/SoC designs do not use all the permissible routing layers for the internal routing corresponding to standard cell connectivity, the proposed STAIRoute framework is not an effective for early global routability assessment. This leads to improper utilization of routing area, specifically in higher routing layers with fewer routing blockages, as the lack of placement of standard cells does not facilitates any routing of their interconnections.

This paper presents a generalized model for early global routability assessment, HGR, by utilizing the free regions over the blocks beyond certain metal layers. The proposed (hybrid) routing model comprises of (a) the junction graph model in STAIRoute routing through the block boundary regions in lower routing layers, and (ii) the grid graph model for routing in higher layers over the free regions of the blocks.

Experiment with the latest floorplanning benchmarks exhibit an average reduction of 4%, 54% and 70% in netlength, via count, and congestion respectively when HGR is used over STAIRoute. Further, we conducted another experiment on an industrial design flow targeted for 45*nm* process, and the results are encouraging with 3X runtime boost when early global routing is used in conjunction with the existing physical design flow.

Additional Key Words and Phrases: Early global routing, hybrid routing model, over-the-block routing, grid graph model, pin access problem.

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1 INTRODUCTION

Integrated circuit (IC) design for very deep submicron (VDSM) fabrication processes requires multiple iterations, mainly during placement and global/detailed routing or even during post-routing optimization, in order to minimize the routing violations due to several lithographic issues as well as failure to conform to specified performance metrics such as power and speed due excessive

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wirelength and via count. In the existing physical design (PD) flow [36] (see Fig. 2 (a)), global routing [9, 13, 24, 27, 33, 35, 36, 42] plays a crucial role for obtaining an acceptable routing solution with minimal/no structural and functional violations. As per this design flow, global routing is traditionally performed, after the placement stage, on a set of nets that define the interconnections between a set of macros and standard cells in the design.

The global routing model identifies the shortest routing path of a net between the center of a bin to the center of another bin only, which contain the corresponding pins of the net. Hence, no local (intra-bin) routing, connecting a net pin contained in the bin with the bin center, is performed at this stage of the design flow and is pushed to detailed routing stage. This is commonly known as pin access problem [7]. Few instances of the local/intra-bin routing problem is illustrated in Fig. 1 where the dotted lines in the zoomed-in routing bins denote the missing local/intra-bin routes that were skipped during the global routing stage. This problem may have significant impact on the overall wirelength of the nets, while lack of local congestion estimation within a routing bin and the number of vias required during detailed routing can grossly impact a successful routing closure. Several errors due to design for manufacturibility (DFM) [12] continue to become more critical as the technology nodes gradually shrink, specially due to local routing and congestion hotspots, in addition to severely impacting the speed and power budget. In order to minimize the design iterations, several interleaved global and detailed routing methods such as [8, 11, 16, 41, 43, 44] have been proposed, in addition to integrated placement and global/detail routing frameworks [26, 28, 33, 34, 38] for incremental improvement of the routing solution and faster routing convergence with minimal violation of structural rules and functional specifications.

Evidently, all the global routing engines start with an initial placement solution, while iterative placement refinements are done using faster feedback from global/detailed routing engines. No such significant effort has been made for iterative floorplan refinement based on some *early routability estimation* on the floorplans, until recently STAIRoute [19] was proposed. This framework provides an insight into the routability of a given floorplan by obtaining an early global routing solution in terms of routing completion, routed wirelength, via count and congestion. These results can be helpful, alike the existing placement and routing framework, in facilitating iterative floorplan refinement as well as guiding the subsequent placement and routing, as per the proposed PD flow illustrated in Fig. 2 (b) (also see how this flow has been adapted to Fig. 10 in Section 3 for an industrial case study).

1.1 Early Global Routing in a Floorplan

Recently, an effort has been made in assessing early routability of a floorplanned layout by STAIRoute [19], using recursive floorplan bipartitioning [20, 21, 23, 29] results that identifies a set of monotone staircases in a floorplan as the routing regions. The capacity of these routing regions is obtained from the net cut information of the corresponding node in the bipartitioning hierarchy (MSC tree [23]). Shortest routing path for a net is identified through these regions assigning the net segments on multiple metal layers depending on the congestion scenario. As cited earlier, these nets were abstracted at the floorplan level and do not account for standard cell connectivity, due to nonavailability of the placement information available for these cells at the floorplanning stage. Instead, these nets define the interconnection between a set of macros (hard blocks) and soft blocks (a cluster of standard cells). In STAIRoute [19], the pin access problem was inherently addressed at the floorplan level, by suitably defining a set of pin-junction edges in the corresponding routing graph (GSRG). These edges facilitate well-defined routing paths between a pin (terminal) of a net to a T-Junction defined in the floorplan [37] by the floorplan bipartitioning results.

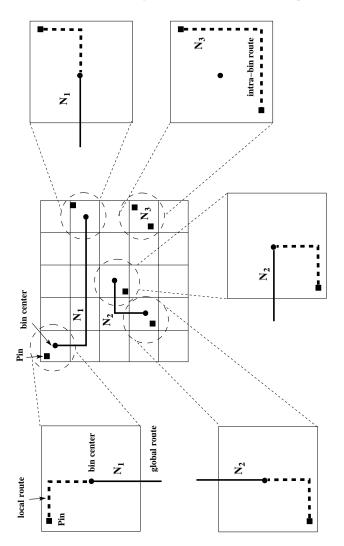


Fig. 1. Post-placement global routing (solid lines) and intra-bin/local routing (dashed lines)

Although STAIRoute [19] is shown to identify a multi-layer routing path of the nets in a floorplan, the corresponding paths are confined in the free regions bounded by the block boundaries only. These regions are identified as monotone staircase routing regions [20, 29]. However, there exist many free routing regions over the macros or the soft blocks (a cluster of highly connected standard cells) over specific routing layers depending on their internal routing, i.e., a block b_i can have free space over a specific routing layer M_i where M_i layers are used for its internal routing. Utilization of these free spaces may improve the routing performance in terms of wirelength, congestion and via count as well as design for manufacturability issues such as *edge placement error* (EPE) [30]. At floorplan level, not all the blocks, specially the soft blocks which are basically a cluster of standard cells based on functionality or higher degree of connectedness, come with the number of metal layers used for their respective internal routing. These internal routing for standard cell connectivity are realized traditionally during post-placement routing. Additionally, the

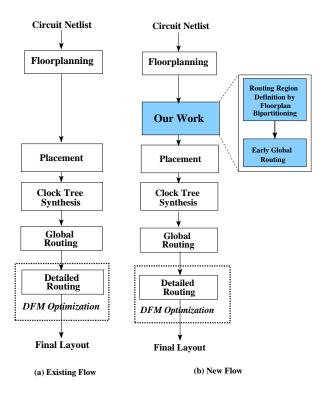


Fig. 2. VLSI physical design (PD) flow: (a) Existing, and (b) Proposed (aligned with this work)

lack of placement information of the standard cells during floorplanning leads to an abstraction of the original netlist barring the connectivity to the standard cells. This yields a subset of the original netlist that define the interconnections between a set of macro (hard) blocks and a set of soft blocks only. Moreover, the nets abstracted at the floorplan level are basically much larger nets if all nets are considered that that connect to both macros (including IO pads) and standard cells, as compared to the nets that connect to only the standard cells. Typically the standard cell only nets and also segments of the nets that connect standard cells and macros are masked by the soft blocks. In any case, the early global routing framework always deal with relatively larger nets using multiple routing layers. Therefore, it is reasonable to realize these early methods for assessing the routability of a floorplan which subsequently guides the placement optimization. Intuitively, this early routing results will help in faster convergence of timing driven placement optimization and subsequent global/detailed routing. We see some relevant results of industrial case study presented in Section 3.

In STAIRoute [19], all the blocks are treated as a set of routing blockages present in all available metal layers. Hence, the routing path of a net is restricted in the monotone staircase regions only, which are located in the adjoining boundary regions of the macros and soft blocks. This routing method uses specified routing layers depending on the vertical/horizontal orientation of the segments in these routing regions. Intuitively, this routing method can be effective when there are fewer number of nets at the floorplan abstraction level interconnecting the macros and soft blocks only, as compared to the original flat netlist seen at the top level that define the connectivity between the macros and standard cells. In practical designs, a macro block usually occupies some, if not all, of the permissible metal layers for routing the nets internal to it; starting from layer M_1 up

to a layer say M_j below the maximum permissible metal layer M_{max} . Therefore, the routing layers $\{M_1 \cdots M_j\}$ in the regions over the planar boundary of these macros are blocked for routing the nets, while $\{M_{j+1} \cdots M_{max}\}$ layers may be available using horizontal/vertical routing segments. This is also applicable to a soft block due to the routing of its internal nets, apparently blocking a number of metal layers say $\{M_1 \cdots M_k\}$ ($M_k < M_{max}$). As cited earlier, floorplan level prior intra-block routing in any soft block is not done due to the lack of placement information of the standard cells in it. Therefore, no *over-the-block* routing is permitted over the soft blocks in these layers. With the increased design complexity, a large number of nets using the same number of routing layers needs to be routed with minimal wirelength and via count during early global routing in a floorplan, over-the-block early global routing of the nets in a floorplan becomes a necessity.

1.2 Major Contributions of this work

In this paper, we present a new early global routing framework called *HGR* in order to realize early global routing of a set of nets in a given floorplan, facilitating *over-the-block* routing of the (sub)nets in the upper metal layers and the routing through monotone staircase routing regions are done in lower layers. As discussed earlier, the internal routing within each block reserve up to a particular routing layer say M_j , while HGR utilizes the free space between the boundary regions of the blocks up to M_j and over the blocks above M_j by proposing a novel 3D hybrid routing graph. In this graph, the lower layers use the floorplan bipartitioning results, while the upper layers use a modification of the existing grid graph model adapted for floorplans. Like in STAIRoute, this routing model aims to address the pin-access (local/intra-bin) problem by suitably defining a set of relevant edges in this graph. Here, M_j will define the maximum layer already used by all the macros for their internal routing, while the soft blocks will reserve the metal layers up to M_j for their internal routing to be done after the traditional placement of the standard cells is done by the existing design flow (refer to Fig. 2 (b)). Therefore, the routing of the nets internal to the soft blocks defining the interconnection of the standard cells is beyond the scope of this work.

A comparative example presented in Fig. 3 gives an idea of the proposed work against STAIRoute. This example shows that, in all layers, STAIRoute confines the nets through the staircase routing regions only, while HGR can use both the staircases as well as the free regions above the blocks. It can be noted that if layer $M_j + 1$ and above are uniformly free for routing over all the blocks, the staircase regions prevalent up to M_j cease to exist. In this regard, the grid graph model becomes relevant and hence used in our hybrid routing model.

We organize the rest of this paper as follows: the proposed early global routing approach HGR in the floorplans is described in Section 2 for over-the-block routing in a floorplan and also explores the scope of exploring an early abstraction of EPE into the routing penalty for obtaining an EPEaware early routability assessment method. Experimental results and relevant discussions appear in Section 3, along with concluding remarks in Section 4.

2 THIS WORK: A GENERALIZED MODEL FOR EARLY GLOBAL ROUTING

In this section, we discuss the proposed early global routing framework for obtaining *over-the-block* routing of the nets in a floorplan, beyond a certain metal layer M_j , while the early routing approach below this layer is similar to that proposed in [19]. We consider a scenario when a macro (or soft block) allows early global routing paths for a set of nets over it beyond some specified metal layer say M_j , using layer $M_j + 1$ up to M_{max} . In this framework, the routing up to M_j is done through the monotone staircase regions similar to STAIRoute i.e. in $\{M_1 \cdots M_j\}$ layers while the grid graph model [36] is used to obtain the over-the-block routing in the subsequent layers

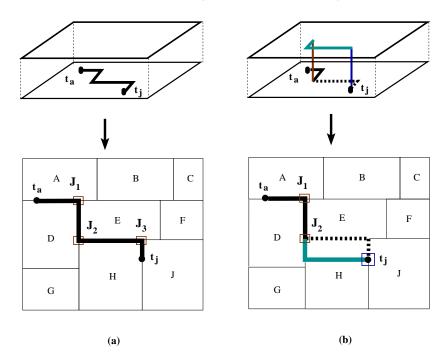


Fig. 3. Instances of 2-terminal net (t_a, t_j) routing using: (a) monotone staircase regions only similar to [19], and (b) both monotone staircase routing in (M_1, M_2) pair and over-the-block (over *H* block) routing in M_3 and above

 $\{M_{j+1}\cdots M_{max}\}$. In fact, STAIRoute can be seen as a special case of this work when M_j is equal to M_{max} , thereby prohibiting the over-the-block routing in any metal layer.

In this work, we adopt a slightly different variant of the existing grid graph model along with the junction graph model presented in STAIRoute [19]. The grid graph is overlaid on the junction graph to form a hybrid graph model. Alike in STAIRoute the global staircase routing graph (GSRG) obtained by augmenting the junction graph for each net, this multi-layer hybrid routing graph model is also augmented for each net before identifying the shortest routing path through multiple metal layers using reserved layer model. Our discussion starts with the adoption of the existing grid graph model in this hybrid routing model, followed by the congestion model and the construction of the hybrid routing graph for each net.

2.1 The Grid Graph Model

Alike the existing grid graph based routing model, the input layout with the placement details of the standard cells and macros is divided into *m*-by-*m* global routing bins, where *m* is predefined. In this paper, we obtain the value of *m* based on the number of blocks in the floorplan, irrespective of the floorplan topology or the corresponding bipartitioning results, there by removing the dependency of the layout area on the routing efficiency. The value of *m* is computed as the ceiling of the square root of the number of T-junctions i.e. $\lceil \sqrt{(2n-2)} \rceil$, where *n* is the number of blocks and 2n - 2 is the number of T-junctions in the floorplan [37] (also see Lemma 1 in [19]).

The grid graph $G_g = (V_g, E_g)$ is defined as follows: each bin corresponds to a vertex $v_p \in V_g$ while each edge $e \in E_g$ denotes a pair of vertices (v_p, v_q) such that the bins (g_p, g_q) corresponding to v_p and v_q share a common boundary. Notably, the number of vertices $|V_g|$ and edges $|E_g|$ can

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be obtained as m^2 and 2m(m-1) respectively. Hence, both these parameters depend solely on the total number of blocks (macros or soft blocks) n in a given design, not on a particular floorplan topology.

LEMMA 2.1. For a given floorplan with n blocks, the grid graph G_q can be constructed in O(n) time.

PROOF. It is evident that for a layout partitioned into *m*-by-*m* routing bins, there are $O(m^2)$ vertices and also $O(m^2)$ edges in the grid graph G_g . Hence, its construction takes $O(m^2)$, i.e., O(n) time.

As discussed earlier, the edge capacity in a planar grid graph model is obtained based on the planar routing blockages in the lowest routing layer pair (M_1, M_2) . They are projected on the routing layers beyond M_2 based on the technology defined routing track pitch and metal width. In our version of grid graph model, the routing capacity of each edge *e* is computed based on the fact that if the corresponding boundary between the designated pair of tiles is fully or partially contained within the bounding box of a net n_i , it accounts for a capacity of 1. This is due to the fact that the net can take have a potential routing path through any of these bins, contained within the bounding box of the net [25, 40]. In this way, the capacity of all the edges is computed for all the nets $N = \{n_i\}$ before the routing process starts. The routing of net (segments) using this grid graph model is done by only L/Z shape pattern routing between a pair of pins or junctions or even bin centers in layers beyond M_2 .

2.2 The Junction Graph and Congestion Model

We revisit the junction graph $G_i = (V_i, E_i)$ defined in [19] as below:

 $V_i = \{J_p\}$, corresponds to a set of T-junctions, and

 $E_j = \{ \{J_p, J_q\} \mid a \text{ pair of adjacent junctions } \{J_p, J_q\} \text{ containing a vertical/horizontal segment } s_k \text{ of a monotone staircase } C_m \text{ between them} \}.$

The weight of each edge $e \in E_j$ is computed as:

$$wt(e) = length(s_k)/(1 - p_e)$$
⁽¹⁾

where p_e , the *congestion* through the segment s_k between $\{J_p, J_q\}$, is defined as:

$$p_e = u_e / r_e \tag{2}$$

Here $(1 - p_e)$ is defined as the *congestion penalty* on the edge weight for routing a net through e. As stated before, the reference capacity r_e for a rectilinear staircase segment is computed from the net cut information of the bipartitioning results. Before routing, u_e is set to 0 and if a net n_i is routed through the corresponding segment s_k , then u_e is incremented by 1.

A similar routing penalty as per Equation 1 is applied on the edges in the grid graph model adopted in this work. The corresponding length parameter for any edge $e \in E_g$ between a pair of adjacent bins (g_p, g_q) is denoted as length(e) and signifies the distance between the center of the bin pair (g_p, g_q) .

2.3 The Hybrid Global Staircase Routing Graph (hGSRG)

We define the proposed routing graph by overlaying the junction graph G_j and the grid graph G_g obtained for a floorplanned layout. We call this routing graph as *hybrid global staircase routing* graph (hGSRG) $G_r^i = (V_r^i, E_r^i)$. For a given net $n_i \in N$ having t_i pins in it, G_r^i is defined as: $V_r^i = V_j \bigcup V_g \bigcup t_i$, and $E_r^i = E_j \bigcup E_g \bigcup E_{tjg}$

Here, E_{tjg} denotes an additional set of edges between (a) a pin and a junction, (b) a pin and a G-Cell, and (c) a junction and a G-Cell and is denoted as:

 $E_{tjg} = \{t_i, J_k\} \bigcup \{J_k, g_m\} \bigcup \{t_i, g_m\}$

where, $\{t_i, J_k\}$ denotes an edge between a net pin t_i and a T-junction J_k in lower layer group (M_1, M_2) pertaining to the junction graph G_j ; $\{t_i(J_k), g_m\}$ denotes a vertical edge between a pin t_i (junction J_k) and a G-Cell g_m such that t_i (J_k) in lower metal layer group (M_1, M_2) is located within the planar boundary of the bin g_m . The edges $\{t_i(J_k), g_m\}$ in this hybrid routing model facilitates the local routing (pin accessibility) within the bin. The steps for the construction of the proposed routing graph hGSRG is illustrated in Fig. 4.

2.4 Local/Intra-bin Routing

Another important aspect of this framework is the routing demand within a bin, i.e., local congestion computation based on the proposed local resource reservation (similar to track reservation [39]). Since the routing capacity and demand are the parameters related to bin boundary edges, these local routes are not entitled to utilize them as per the existing grid graph model. On the other hand, our routing model allows us to use grid graph edges for routing the nets beyond some specified routing layers such as M_3 beyond the layers used for monotone staircase routing such as (M_1,M_2) layer pair, as well as obtain the local routes within a bin. The grid graph edges are used to route the net segments that were not routed in (M_1,M_2) , but between the centers of the corresponding bins. These net segments may either be between two junctions or between a pin and a junction. Therefore, the remaining bin center to pin (junction) edges are used to move the net segment to upper layers $(M_3$ and above) with an additional via overhead. As mentioned earlier, all the local routes in this work use L-shaped patterns for minimal via overhead. This is illustrated in Fig. 6 (c).

In Fig. 5, we illustrate the routing demand u for each boundary of a bin after local routing of a net is performed within the bin. This example shows that the position of the pin (junction) in one of the four quadrants of the bin and the global route of the net terminating on the bin center determine the reservation of routing demand u of the corresponding boundary edges; example (a) shows that unit routing demands in the top and left edge are reserved for local routing while bottom edge demand is meant for global route, (b) uses the same like in (a) but with right edge for global route. The example of (c) and (d) are special cases that are closely related to the edge being used for global route with respect to the position of the pin (junction). While the local routing instance in (c) shows that it utilizes the same left edge capacity for both local route, and the global route segments and top edge capacity for vertical demand of the local route, and left edge for the global route at the top edge share with vertical segment of the local route, and left edge for horizontal segment of the local route. In these cases, no other edge capacity is relevant and hence not reserved as dictated by zero values in the demand in these edges. In this example, we also note that the wirelength is further minimized (as dictated by the arrow and the dotted line) due to common segment length between global and local routes.

2.5 Illustration of the proposed routing method

We illustrate the working of the proposed early global routing method HGR in Fig. 6 using a 2terminal net (t_a, t_j) . In this example, we assume that this routing method considers only (M_1, M_2) pair for routing through the monotone staircase regions only, due to the inherent routing blocks due to the macro/soft blocks. As in Fig. 6 (a), there are two routing paths between the terminal pair:

(i) as per STAIRoute [19] obtains $(t_a, J_1, J_2, J_3, t_j)$ of the net is entirely confined within the monotone

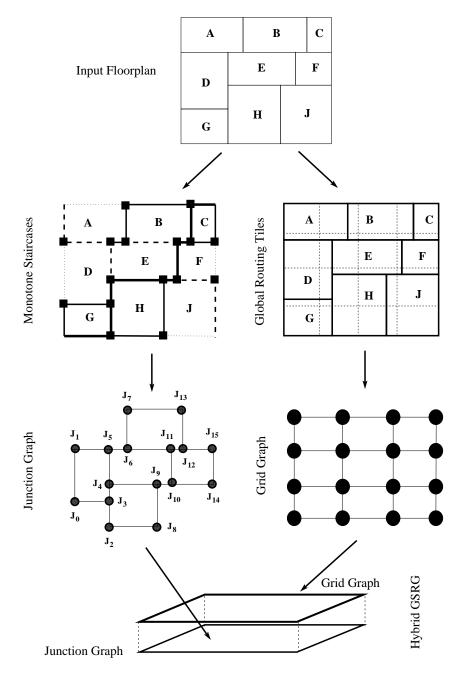


Fig. 4. Construction of hybrid Global Staircase Routing Graph (hGSRG)

staircase routing regions, i.e. through the boundary regions, as denoted partially by black solid line as (t_a, J_1, J_2) and dashed line (J_2, J_3, t_j) . This is also illustrated earlier in Fig. 3 (a) by an entirely solid poly-line, by visualizing the dashed poly-line as solid.

(ii) here dotted line is used to denote illustrated that this path is congested in lower metal layer

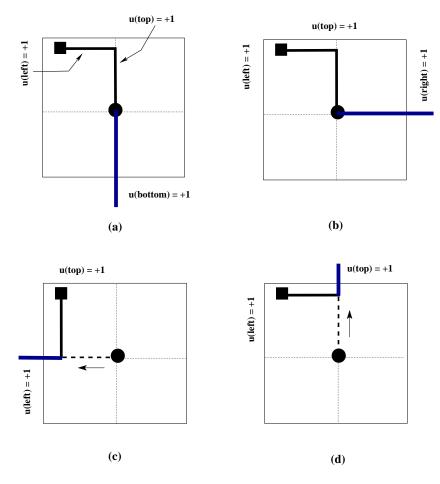


Fig. 5. Instances of local routing within a bin using routing demand reservation: (a) - (d) enumerates the instances of a fixed pin location vs. bin-to-bin grid routing (in blue)

pair say (M_1, M_2) and this framework is capable of finding an alternative path through the higher routing layers (say M3 and above), but over the block H. Notably, STAIRoute would route the partial routing segment, denoted as the dashed line (J_2, J_3, t_j) , in higher layer pairs say (M_3, M_4) . This is due to the fact that its routing model is based only on the Junction graph model which allows routing through the monotone staircase boundary regions only.

Despite that, both the routing paths incur same wirelength and via count for same number of layer switch, providing more options of alternative routing paths without having any additional routing cost. On the contrary, if STAIRoute is not able to route along (J_2, J_3, t_j) in either M_3 or M_4 or both due to prevailing congestion scenario, subsequent permissible layer(s) and hence more vias will be used for this interconnection. But HGR will use the free region over the block H in (M_3, M_4) layer pair only. This implies that fewer metal layers may be used by HGR for overall routing completion as compared to STAIRoute.

For utilizing the free space over the block H, Fig. 6 (b) shows how this hybrid routing graph model helps in identifying the remaining routing path $(J_2 \rightsquigarrow t_j)$ through the routing bins in upper metal layers (M_3, M_4) with the help of the grid graph model used in it. Although, the grid graph

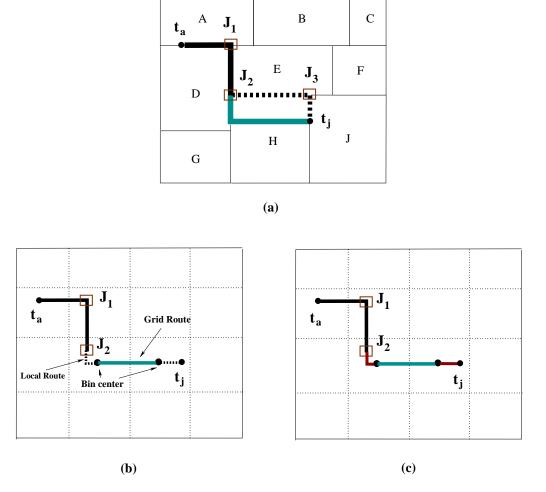


Fig. 6. Early global routing of 2-terminal net (t_a, t_j) : (a) monotone staircase routing (partly dotted) and overthe-block routing (over *H* block), (b) directional routing between bin centers, and (c) local routing for the pin t_j and the T-junction J_2 with the corresponding bin centers

model obtains a routing path between the centers of a pair of bins, where one bin belongs to J_2 while the other contains t_j . Till now, the routing between the respective bin centers and $J_2(t_j)$ are not done. This is an example of pin-access problem, also commonly known as intra-bin or local routing problem. The third instance in Fig. 6 (c) shows the local routing between J_2 with one bin center and t_j with the other bin center, both are done in (M_3, M_4) pair, with the help of the corresponding pin/junction to G-Cell edges (in $\{t_i, g_m\} \bigcup \{J_k, g_m\}$).

2.6 The Algorithm: HGR

In Algorithm 1, we summarize the steps for the proposed early global routing method *HGR* (*Hybrid Global Router*). Similar to STAIRoute [19], Dijkstra's shortest path algorithm [17] is used to identify the shortest routing path of a 2-terminal net (segment) in the proposed hybrid routing graph. We also use a similar multi-terminal net decomposition approach in order to identify 2-terminal

net segments as proposed in [19], for the identification of the Steiner tree topology. The set of nets N are ordered first according to net-degree, and then HPWL in the given floorplan based on the bipartition hierarchy. This algorithm takes the junction graph G_j and the grid graph G_g as inputs which are already obtained using the floorplan bipartitioning results obtained by one of the existing works [20, 21] with suitable trade-off values for minimal bend routing. For multi-terminal nets, we use a multi-terminal net decomposition method similar to that proposed in [19]. According to this method, for each valid terminal pair, i.e., the valid edge in the resulting spanning tree, we apply this two terminal hybrid routing method, followed by Steiner point identification.

	input :Junction Graph $G_j(V_j, E_j)$, Grid Graph $G_g(V_g, E_g)$, an ordered set of nets $N = \{n_i\}$ output :Early global routing of each <i>t</i> -terminal ($t \ge 2$) net $n_i \in N$								
	Initialize routed (unrouted) net count c_r (c_u) to 0								
	for each ordered net $n_i \in N$ do								
3									
4	if n_i is a 2 terminal net then								
5	Identify the shortest routing path using dijkstra single source shortest path algorithm [17] on G	i							
6	if There exists a shortest path then	'							
7	Increment c_r								
8	Compute netlength, and via count								
9	Update routing demand u for each routing resource along this path								
10	end								
11	else								
12	Skip this net and increment c_u								
13	end								
14	end								
15	else								
16	Construct the node graph G_c^i								
17	$T_c^i = \text{MST}(G_c^i)$								
18	for each valid 2-terminal pairs $(t_j, t_k) \in T_c^i$ do								
19	Identify the shortest routing path on G_r^i								
20	if There exists a shortest path for (t_j, t_k) terminal pair then								
21	Compute routed netlength, and via-count								
22	Update routing demand u for each routing resource along this path								
23	end								
24	else								
25	Skip this net and increment c_u								
26	end								
27	end								
28	Increment c_r								
29	Identify the <i>Steiner Point(s)</i> for all two terminal routed net segments								
30	Recompute netlength and via-count for n_i								
31	end								
-	end Compute routing completion (ratio of a , and $ N $) and congrestion (see Eqn. 2) for all the routing regions								
33	³ Compute routing completion (ratio of c_r and $ N $) and congestion (see Eqn. 2) for all the routing regions across the metal layers.								
	Algorithm 1: HGR: An Early Global Router for over-the-block routing in Floorplans								

Algorithm 1: HGR: An Early Global Router for over-the-block routing in Floorplans

After successful routing of a net n_i , the capacity of the corresponding segments in the monotone staircases and grid edges along the routing path of n_i is updated by 1. In this work, we assume that the pins of a block are located in metal layer M_1 or M_2 . The pins residing in lower metal group (M_1, M_2) are associated with the junction graph, as shown in Fig. 6, forming pin-junction edges similar to the graph model used in STAIRoute. The pin-bin and junction-bin edges in G_r^i are constructed by identifying the pins/junctions within the corresponding bin, by overlaying the grid graph on the junction graph. The routing cost of these edges, being the vertical connecting edges between G_j and G_g , is simply the planner length between the pin/junction location and the center of the bin and the number of vias incurred due to routing through multiple layer groups.

Alike the existing post-placement global routers, no capacity constraints for these edges are considered as congestion through these vertical edges has little significance, except via overhead. The main contribution in this work is that we use G_j for identifying the (partial) routing path of n_i in lower group of metal layers such as M_1 - M_2 only, while G_g is used to route those nets in the subsequent higher metal layers beyond M_2 . The routing through the grid graph takes place when a segment of a net cannot be completed in M_1 - M_2 layers, obeying the congestion model in the corresponding rectilinear staircase segments. Although (M_1, M_2) layer pairs have been used in this work, additional layer pairs such as (M_3, M_4) , (M_5, M_6) etc. can be used until (M_{max-1}, M_{max}) . When (M_{max-1}, M_{max}) is also used, this model resembles with STAIRoute leading to no over-the-block early global routing possible in the floorplans.

THEOREM 2.2. Given a floorplan with n blocks and k nets with at most t-terminals ($t \ge 2$), HGR takes $O(n^2kt)$ time for finding the routing path of all the nets.

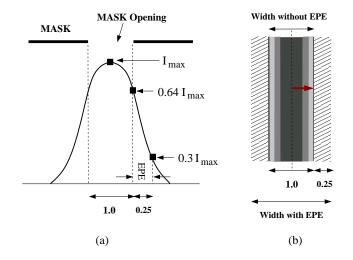
PROOF. For a given net n_i with t pins (terminals), there are O(t) pin-junctions edges as per Lemma in [19]. Again, for m routing bins, with t pins and 2n - 2 vertices in G_j , O(t) pin-bin edges and O(n) junction-bin edges can be obtained. For each net n_i , using Lemma 2, the hybrid GSRG G_r^i construction takes O(t + n), i.e., O(n) time, since t = o(n).

Alike STAIRoute, our implementation of Dijkstra's single source shortest path algorithm takes $O(n^2)$ time. For t(> 2)-terminal nets, both the construction of G_c^i and finding its MST require $O(t^2)$ time (see [19]). Therefore, finding a routing path for a t terminal net requires $O(n + n^2t + t^2)$, i.e., $O(n^2t)$ time. Hence HGR takes $O(n^2kt)$ time for routing k nets.

It is evident from Theorem 2.2 that HGR presented in Algorithm 1 has the same time complexity as that of STAIRoute, with a constant time overhead for the construction of the grid graph and identification of the pin (junction)-bin edges. This also takes into account the routing demand update in each of the edges in the hybrid graph pertaining to both the junction graph and the grid graph, once a net is routed successfully.

2.7 Early Abstraction of Edge Placement Error

In this section, we study how edge placement errors (EPE) [14, 18, 30] occur due to inefficient printability issues of sub-wavelength features using the existing optical illumination system using 193*nm* wavelength. These errors are further aggravated due to the congestion scenario in the routing regions. The intensity map in Fig. 7 (a) depicts that the intensity is not uniform under the mask opening while the same is not zero beyond the mask opening. Therefore, it signifies additional metal width of the wire segment beyond its contour (see Fig. 7 (b)). Thus, if a routing region is more congested, there is little scope to cope up with EPE than doing ripup and reroute for some of the nets (or a part of it), as illustrated in Fig. 7 (b). Moreover, EPE related routing blockage to other nets may leave little room for the detailed routing of the adjacent nets. If this



problem is neglected during the detailed routing stage, it will cause a failure during DFM closure stage.

Fig. 7. Edge Placement Error (EPE): (a) Intensity map vs. mask opening [30], and (b) actual vs. effective metal width with intensity gradient across the normalized width (dark grey to light grey from core to boundary)

The intensity map in Fig. 7 (a) depicts the maximum intensity I_{max} at the center of the mask opening [30] and the intensity falls off gradually in a pattern similar to sinc(x) = sin(x)/x function, where x is the distance measured from the center of the mask opening. Notably, the intensity at the mask boundary (edge) is around 64% of I_{max} . The intensity gradient across the width (dictated by an arrow in Fig. 7 (b)) signifies the intensity deficiency causing optical proximity errors (OPE). In this model, we consider only the EPE effect in our early routing model in HGR due to nonzero intensity beyond mask opening as the OPE effect due to the said intensity gradient can not be modeled without proper simulation or rule definition at this early stage of physical design flow. According to [30], we consider the threshold point for EPE as the point where the intensity falls to 30% of I_{max} , in the region beyond the mask edge, i.e., beyond the wire boundary contour. It amounts to approximately 25% increase in effective metal width on either side of the wire. As a result, it has more interfering effects on the neighboring wire segments of other nets, called EPE induced routing blockage, due to the effect of positive optical interference. This kind of violation due to EPE is discovered during optical rule check (ORC) in the physical verification process of the existing physical design flow. In this case, either wire spreading or rip-up and re-route methods are applied in order to minimize number of such violations.

In order to incorporate this EPE effect in our early global routing framework HGR, we abstract this effect in the routing demand for assessing the congestion scenario in any metal layer at any given routing instance. This early abstraction of EPE into our proposed routing framework HGR has the potential to reduce the lithography hot-spots due to EPE routing blockage (see Fig. 8 (a)) at the smaller technology nodes after the detailed routing stage. Therefore, it will reduce the potential overhead of multiple iterations due to wire-spreading or ripup and reroute (RR) during detailed routing (see Fig. 8 (b)) for EPE hotspor reduction [14, 18, 30]. In the congestion model of HGR, the penalty due to this EPE cost abstraction is incorporated as follows: after each net is routed through the routing region e, its routing demand u_e is incremented by 1.5 considering the effect of additional 25% metal on the either side. After routing a net n_{i-1} , the congestion in the

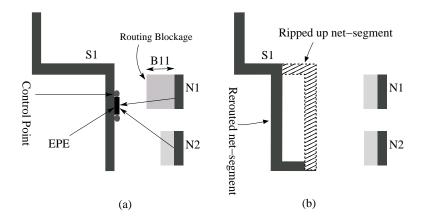


Fig. 8. Routing blockage due to edge placement error (EPE) [30] and Rip-Reroute to alleviate it

corresponding routing resources along its routing path are computed. The routing graph (hGSRG) G_{ri} for the subsequent net n_i is constructed in order to identify the routing path for it along with the present layer wise congestion scenario in the routing regions.

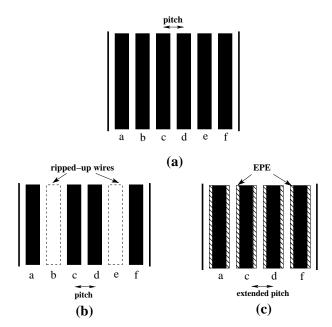


Fig. 9. Wire spacing/pitch modulation for EPE aware early global routing: (a) all 6 tracks used, (b) 2 wires ripped up due to EPE hotspot, and (c) result of EPE aware early global routing

Due to this process, there will potentially be fewer nets to be ripped up aimed at EPE hotspot reduction during post-routing/layout optimization. The example in Fig. 9 (a) showcases this considering six tracks $(a \cdots f)$ for routing the nets, without accounting for EPE effect. However, some of the nets, in tracks *b* and *e* shown in this example, may be ripped up later during EPE aware routing optimization. On the other hand, as depicted in Fig. 9 (c), the proposed EPE aware early

routing framework with *extended pitch*, which accounts for taking u_e as 1.5 for each net routed in region *e* than using 1.0 when EPE is not considered, routes only those nets, such as those remained in tracks *a*, *c*, *d*, *f*, after ripping up the other two nets during the existing methods for EPE hotspot reduction. This example shows that a routing solution considering such an early model may potentially reduce the overhead of multiple iterations due to (i) first routing the nets, and (ii) then ripping some of them up in an attempt towards EPE hotspot reduction.

3 EXPERIMENTAL RESULTS

In this paper, we used IBM HB floorplanning benchmarks [2] presented in Table 1 for verifying the proposed early global routing method HGR presented in Algorithm 1. These benchmarks were derived from ISPD98 placement benchmark circuits with certain modifications [2], in order to form a set of clusters from the standard cells present in the placement benchmark circuits. These clusters not only defined a set of soft blocks, it also helps in defining a subset of the original netlist as the interconnection between the macros and these soft blocks. Notably, these interconnections represent relatively larger nets, some are partial though, barring the standard cell connectivity of the original nets defined in the design. As a result, these modified nets terminate at the boundaries of the macros/soft blocks.

Circuit	#Blocks	#Nets	Avg.	HPWL
Name			NetDeg	$(10^{6} \mu m)$
ibm01	2254	3990	3.94	8.98
ibm02	3723	7393	4.84	22.19
ibm03	3227	7673	4.18	23.83
ibm04	4050	9768	3.92	30.82
ibm05	1612	7035	5.58	18.12
ibm06	1902	7045	4.92	21.78
ibm07	2848	10822	4.44	42.48
ibm08	3251	11250	4.92	46.57
ibm09	2847	10723	4.08	48.35
ibm10	3663	15590	3.85	121.23

Table 1. HB Floorplanning Benchmark Circuits [2]

These floorplan instances were generated using *Parquet* [5, 6] using random seed for each of the circuits, i.e., *ibm*01 to *ibm*10. The proposed algorithm HGR was implemented in C programming language and the experiments were conducted on a Linux platform having Intel Xeon processor running at 2.4GHz and has 64GB RAM in it. Since IBM benchmarks [2] do not provide any pin location details, both STAIRoute and HGR assumed the pins of the blocks connected to the nets at the center of the blocks. A maximum of eight metal layers were permitted to be used for routing the floorplan level nets, using preferred routing directions as horizontal/vertical in odd/even layers. It is also assumed that only two metal layers (M_1 and M_2 only) out of all the available layers were reserved for internal routing of the macros/soft blocks. For fair comparison, we reran STAIRoute [19] with these benchmarks, as the results reported in [19] were obtained for much smaller floorplanning benchmark circuits [5].

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3.1 Comparison with Existing Early Global Router STAloute

First, we present a comparative study between the experimental results obtained by HGR and STAIRoute [19]. In this comparison, we consider both with and without abstracted EPE cost in the congestion model (see Eqn. 1), discussed in the previous section. With these experiments, our aim is study the effectiveness of the proposed generic early global routing framework, which supports over-the-block routing beyond some predefined routing layer, with respect to the existing work STAIRoute [19]. In addition to that, we also aimed to incorporate an early abstraction of EPE cost in the routing penalty for both HGR and STAIRoute, as outlined in [22] and also presented in the previous section in details. The corresponding results are presented in Table 2, for (a) netlength, (b) via count, and (c) average worst congestion [39].

These results were obtained for 100% routing completion of the nets using up to eight routing layers, ensuring no over-congestion as per the congestion model defined in Eqn. 1. The results obtained for netlength shows almost identical values obtained by these early global routers for both without and with EPE cost in the routing penalty; HGR shows a slight improvement with an average of 3.5% and 4.5% reduction in wirelength over STAIRoute for both with and without EPE cost respectively. Although both these routers tend to confine the routing paths within the bounding box using one/two/more bends (monotone patterns), the overall netlength varies due to the non-overlapping (non-common) wire segments through the same or different metal layers, as obtained by the multi-terminal net decomposition method (see [19] for details). This is apparent as HGR has fewer layer change due to over-the-block routing approach, while STAIRoute uses more layer changes while confining the routing path through the monotone staircase boundary regions only. Accordingly, via count for HGR also shows significant average reduction of 53% and 54.5% respectively over STAIRoute for both the cases, due to fewer layer changes among the wire segments of a net or subnet.

Circuit	t Length $(10^6 \mu m)$		Via Count(10 ⁵)				Worst Avg. Congestion (wACE4)						
Name	STAIRo	ute [19]	HO	HGR S		STAIRoute [19]		HGR		STAIRoute [19]		HGR	
		+EPE		+EPE		+EPE		+EPE		+EPE		+EPE	
ibm01	11.44	11.47	11.35	11.16	2.16	2.19	1.08	1.05	0.750	0.282	0.101	0.146	
ibm02	32.18	32.27	30.73	31.26	6.17	6.28	2.82	2.79	0.917	0.294	0.100	0.135	
ibm03	35.60	35.84	32.08	33.95	5.44	5.59	2.42	2.43	0.935	0.714	0.104	0.128	
ibm04	39.13	39.23	39.58	37.95	7.20	7.30	3.33	3.25	0.524	0.786	0.115	0.138	
ibm05	26.43	26.45	25.94	25.73	4.01	4.06	2.08	2.11	0.203	0.277	0.108	0.158	
ibm06	31.20	31.24	30.72	30.80	4.27	4.33	2.12	2.14	0.773	0.955	0.124	0.154	
ibm07	56.70	56.80	56.44	54.72	7.83	7.93	3.61	3.51	0.244	0.320	0.094	0.120	
ibm08	67.81	68.06	62.78	64.64	9.35	9.52	4.09	4.21	0.647	0.569	0.082	0.117	
ibm09	63.66	63.79	62.15	61.13	7.08	7.17	3.28	3.22	0.789	0.750	0.103	0.136	
ibm10	153.37	154.04	141.01	133.30	10.70	11.02	4.90	4.74	0.249	0.575	0.110	0.156	
Norm. Geo. Mean	1.000	1.003	0.964	0.957	1.000	1.017	0.470	0.465	1.000	0.948	0.197	0.259	

Table 2. Comparing the Routing Results (with and without EPE cost)

In this table, we also present the congestion values measured as the worst average congestion in terms of a parameter called *wACE4*, showing an average reduction of 73% to 80% in case of HGR as compared to that in STAIRoute, in both cases of with and without EPE cost. In this paper, the congestion analysis is motivated by the approach proposed in GLARE [39]. The authors in [39] defined a parameter called ACE(x) (Average Congestion on Edges) computed for the worst x% congested edges among all routing layers and the prescribed values of x are one of the values belonging to {0.5, 1, 2, 5}. In our analysis, we compute an average of ACE(x) for all the prescribed x values and term it average worst congestion wACE4. This congestion analysis shows that HGR considers a more realistic approach similar to that adopted to by the post-placement global routing methods, while STAIRoute assesses only congestion in the regions designated as the monotone staircase boundary regions in the floorplan. The congestion values obtained by STAIRoute and hence HGR for lower layers is justified for the lower layer pair (M_1, M_2) due to the assumption that a very small fraction of of the total layout area is available as the effective routing space, because of the routing space reservation for internal routing in the soft blocks and also the macros whose internal routing has already been done using these two layers. As per this assumption, layers beyond M_2 have plenty of free space of the blocks which are effectively used by HGR, while STAIRoute can not use those free space because of its routing model.

Circuit		#Routing	-layers		CPU time (sec)				
Name	STAIR	oute [19]	H	GR	STAIRoute [19]		HGR		
		+EPE		+EPE		+EPE		+EPE	
ibm01	6	8	4	4	2.822	2.763	10.273	10.479	
ibm02	6	6	4	4	16.359	17.144	63.529	69.391	
ibm03	6	6	4	4	10.884	11.655	43.393	47.748	
ibm04	6	6	4	4	21.364	23.454	90.265	81.634	
ibm05	6	6	4	4	2.799	2.841	11.375	11.502	
ibm06	6	8	4	6	3.673	3.787	14.915	15.311	
ibm07	8	8	6	6	12.163	12.423	51.911	50.152	
ibm08	8	8	6	6	18.102	18.087	76.065	73.402	
ibm09	8	8	6	6	11.281	11.360	46.418	47.728	
ibm10	8	8	6	8	26.387	27.888	126.338	126.978	
Norm.									
Geo.	1.000	1.029	0.700	0.749	1.000	1.032	4.114	4.157	
Mean									

Table 3. Number of Routing Layers and CPU time (sec) for routing

Table 3 presents the number of metal layers used out of maximum permissible 8 layers and the runtime for routing in seconds, for STAIRoute anbd HGR using both with and without EPE costs. These results show that the number of routing layers used for each circuit in case of HGR are 25 - 30% fewer than that for STAIRoute, considering all the cases. One notable point here is that, for both HGR and STAIRoute, slightly higher number of layers are required in order to obtain 100% when EPE cost is incorporated in the routing penalty. Lastly, as discussed earlier in this paper (see Theorem 2.2), the results also show that HGR needs approximately a constant 4X more runtime over STAIRoute to route the same set of nets for the same floorplan instance.

3.2 Comparison with Post-placement Global Routers

In Table 4, we present a comparison of the normalized netlength for some of the existing postplacement global routers [10, 13, 31, 32, 35, 45] and the proposed early global routing methods STAIRoute and HGR, based on the corresponding benchmark circuits. Notably, the results for the existing global routers were obtained on IBM ISPD98 placement benchmarks, while HGR and STAIRoute [19] obtained the corresponding results on IBM-HB floorplanning benchmarks derived from it [2]. As cited earlier, a floorplanning benchmark is obtained from a placement benchmark circuit using suitable clustering algorithm, the IBM-HB floorplanning benchmarks were derived from the ISPD98 placement benchmarks [2]. This conversion incurs significant information loss due to standard cell clustering and the corresponding netlist modification. Therefore, it is unfair to compare the actual netlength obtained for the respective circuits by both the frameworks. Instead, the netlength obtained for each circuit is normalized with respect to the respective Steiner length Table 4. Normalized (w.r.t Steiner length [15]) netlength between the existing Global routers and early global routing methods STAIRoute [19] and HGR

Circuit		Post-pl	acement	Early Global Routers				
Name	$[32]^{b}$	[13] ^b	[45] ^b	[35] ^b	[31] ^b	$[10]^{b}$	STAIRoute[19] ^c	HGR ^c
ibm01	1.071	1.042	1.068	1.053	1.059	1.039	1.156	1.147
ibm02	1.036	1.032	1.038	1.018	1.027	1.024	1.175	1.121
ibm03	1.007	1.007	1.007	1.005	1.010	1.005	1.175	1.059
ibm04	1.045	1.028	1.046	1.027	1.045	1.023	1.155	1.169
ibm05 ^d	-	-	-	-	-	-	1.198	1.176
ibm06	1.011	1.007	1.013	1.006	1.013	1.007	1.166	1.148
ibm07	1.018	1.006	1.015	1.007	1.016	1.007	1.192	1.187
ibm08	1.005	1.008	1.009	1.006	1.010	1.006	1.197	1.109
ibm09	1.007	1.006	1.009	1.004	1.011	1.008	1.199	1.171
ibm10	1.016	1.027	1.015	1.008	1.020	1.010	1.187	1.200
Average	1.024	1.018	1.024	1.015	1.024	1.014	1.180	1.149

b - using ISPD98 global routing benchmarks, c - using IBM-HB floorplanning benchmarks, and d - no result on ibm05 of ISPD98 benchmark by the existing global routers

computed by Flute [15]. The results in this table for both STAIRoute and HGR are slightly higher as the nets are routed through the monotone staircase routing regions only for STAIRoute in all the routing layers, while HGR incurred sightly lower netlength value than STAIRoute due to the proposed over-the-block routing approach. However, as we pointed out earlier, the post-placement routers considered all the nets, including the standard cell connectivity, unlike STAIRoute and HGR. Moreover, both STAIRoute and HGR addressed intra-bin/local routing for pin accessibility at the floorplan level, unlike in post-placement global routing which push the pin-accessibility issue to the detailed routing stage. In summary, the main purpose of this study is to understand how these early global routing approaches can assess initial routing metrics like netlength while ensuring 100% routing completion, in terms of the deviation of the overall netlength from the Steiner length without considering any routing blockage. The results show that HGR and STAIRoute deviate 18% and 14.5% from their respective Steiner length, for the corresponding floorplan instances of each circuit. This implies that there is a scope of improvement in the floorplan topology, such as clustering of standard cells and most importantly the locations of the macros/soft blocks), for enhancing the routing performance by using these early routing results in floorplan optimization tools such as Parque [5].

In the post-placement global routing framework, congestion analysis is done by the number of overflows in the routing edges. On contrary, we used a relative congestion metric (see Eqn. 2) inspired by GLARE [39]. In this work, we adopted a congestion analysis method using the parameters defined in [39] as our congestion model (see Eqn. 1) does not allow overflow (routing demand exceeding the routing capacity) based computation. Due to this reason, we could not make any direct comparison on congestion overflow for each circuit. Later in this section, we present some overflow based congestion results obtained for some industrial design inputs by an industrial tool which reports both versions of congestion analysis. We also skip the comparison for via counts as both these frameworks are in different scope of operation as per the PD flow. In this comparison, we used only ISPD98 benchmarks whose corresponding IBM-HB floorplanning benchmarks [2] are the latest ones available for academic research. We are not able to compare the routing results for the latest ISPD07/08 global routing benchmarks, since the corresponding floorplanning benchmarks are not available online. In order to study the effectiveness of the proposed early global routing method HGR with respect to the existing post-placement global routing paradigm, we subsequently present a case study with a well known industrial physical design (PD) tool.

3.3 An Industrial Case Study

In order to study the impact of early global routing presented in this work (also in [19] on the existing physical design flow, we conducted an industrial case study by developing a framework that can integrate HGR (and also STAIRoute) with industrial PD tool *Olympus-SoC* [4], as outlined in Fig. 10. This framework consists of an interface for industry standard LEF/DEF exchange format between STAIRoute/HGR and Olympus tool. In this study, we used a design to be implemented with a 45*nm* physical design library [3], while the physical verification was done by Calibre tool suite [1].

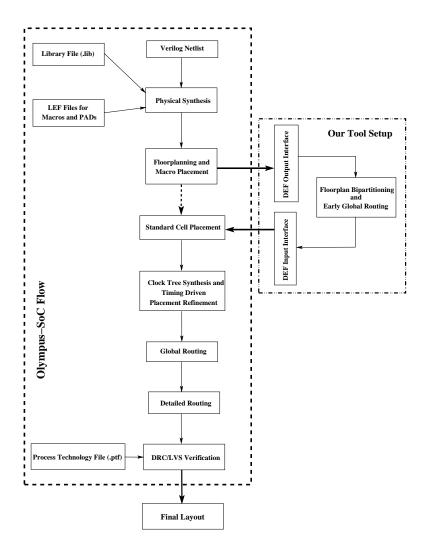


Fig. 10. Modified Olympus-SoC [4] Physical Design (PD) flow with integrated Early Global Routing (HGR and STAIRoute [19])

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Parameter(s)	Olympus-SoC [4]	Olympus [4]	Olympus [4]
		+ STAIRoute [19]	+ HGR
Standard Cells (Macros)	16360 (4)	16611 (4)	16504 (4)
Nets	16474	16725	16618
Buffer/Inverter	225/6527	225/6575	225/6441
Placed Area (Buf area) (μm^2)	45909 (10104)	45966 (10157)	45834 (10018)
Utilization (%)	59.17	59.24	59.07
Wirelength(mm)	273.02	273.52	273.43
Via Count (x10 ³)	52.80	53.13	52.84
WNS/TNS (ns)	0.00/0.00	0.00/0.00	0.00/0.00
Avg. Congestion (X/Y)	0.123/0.111	0.122/0.112	0.122/0.112
Worst Congestion (X/Y)	0.826/0.928	0.791/0.916	0.782/0.909
Edge Overflow (X/Y)	0/0	0/0	0/0
DRC/LVS violations	No	No	No
# of Routing Layers	8	8	8
CPU time (sec)	1979	688	699

Table 5. Impact of early global routing on Olympus PD flow [4]

In this exercise started with a floorplan instance of a design generated by Olympus-SoC tool. Default placement constraints were used for the subsequent placement engine and the design utilization target was set at 60%. Subsequent stages in Olympus implemented the design as per Fig. 10, having no early routability assessment done on the floorplan. In another attempt, STAIRoute/HGR obtained the same floorplan instance through the LEF/DEF interface and obtained the early global routing solution for randomly chosen (γ , β) values such as (0.5, 0.2) used to obtain the recursive floorplan bipartitioning results [20] and define the routing regions. For routing, we used 10 metal layers using preferred routing directions in each layer, horizontal being on the odd layer and vertical on the even, as supported by the given technology. In this study, we emphasized on timing driven placement and hence on parameters like TNS/WNS. Using both the approaches in Olympus, i.e. with and without early global routing, we obtained the final layout with no DRC/LVS violations, and also ensured zero timing violations in terms of non-negative WNS/TNS values. We used all other default values pertaining to Olympus-SoC tool for this exercise and noticed that timing was given more priority, than congestion/via minimization, using buffer insertion. This is the reason that Olympus tool used more buffer/inverter cells when STAIRoute was used. Hence more number of nets were introduced during timing driven standard cell placement, after early global routing (see Fig. 10 (b)). In all the cases, the target of 60% placement density (utilization %) was met while no timing violations were reported, and non-negative WNS/TNS values were achieved subsequently. It is important to note here that, the present day design philosophy goes for fixed outlined layout with predefined layout area. Therefore, higher utilization value may sometime lead to infeasible, sometimes incomplete, routing solution due to either (i) maximum usage of higher number of layers, and (ii) even the maximum number of layers permissible by the technology is not sufficient.

The corresponding results are presented in Tab 5 for the given floorplan instance. For the results pertaining to early global routing, important observations can be made in worst/average congestion (in X/Y direction), via count, runtime and even timing despite insignificant increase (less than 1%) in cell and net count due to timing driven placement of standard cells by Olympus with early global routing than in standalone Olympus mode. Moreover, no DRC/LVS violations nor placement density constraint violations (utilization $\neq 60\%$) were noticed. Runtime for Olympus with STAIRoute/HGR is significantly improved due to fewer number of iterations in order to converge

on an acceptable routing solution with no timing violations, being roughly three times faster than that for standalone Olympus, while results for HGR+Olympus are shown to be the best among all. Moreover, significant runtime improvement for the entire flow can also be noticed due to fewer number of iterations, as the timing driven placement optimization appears to have been guided by the early global routing results for both HGR and STAIRoute.

4 CONCLUSION

In this paper, we present a new early global routing framework that facilitates over-the-block early global routing of the nets in a given floorplan. In this work, layer M_2 is assumed to be the maximum routing layer used for internal routing for macros/soft block. While STAIRoute [19] identifies the routing paths of the nets through the monotone staircase routing regions in all routing layers, the proposed method HGR routes the nets through these regions only in lower metal layers (M_1 , M_2). For higher routing layers, i.e. beyond M_2 , HGR uses the free space over the blocks for routing the nets or parts of the nets. Alike STAIRoute, this model also attempts to address the pin access problem at the floorplan level by suitable edge definitions in the proposed hybrid routing graph, as presented in Section 2. Therefore, HGR can be seen as a generic version of STAIRoute. If the maximum layer assumed to be reserved for internal routing is taken as the maximum allowable routing layer, then there will be no free space of over the macro/soft blocks. This implies that all the nets are to be routed through the monotone staircase regions situated at the boundary regions of each of the blocks, and applicable for all layers.

Experimental results presented in Section 3 show that HGR obtains smaller wirelength, fewer via count and also less congestion as compared to STAIRoute, with a more realistic early global routing approach by obtaining over-the-block routing paths beyond a specific routing layer. These results also ensure that the congestion values are constrained to 100% as per the proposed congestion model, with 100% routability. A comparison with the existing post-placement global routers also show that, even without detailed placement of standard cells, the proposed early global routing approach HGR can have a good idea of routability, wirelength and congestion values in a given floorplan instead of using primitive metrics like half perimeter wirelength (HPWL) and pre-routing probabilistic congestion analysis. The industrial case study also indicates the potential of early global routing framework in guiding acceptable final routing solutions in fewer iterations, and with fewer/no violations due to design for manufacturibility issues and also leverage on minimalistic compromise on the performance metrics like speed, within a competitive time frame.

Based on the results from the industrial case study, we plan for a new placement and routing framework guided by this generic early global routing method for a given floorplan solution and subsequently incorporate the DFM issues with enhanced models using extensive simulations results for smaller VDSM process nodes. We also plan to explore the scope of this work in 3*D* IC design flow.

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