A Formal Approach for High Level Synthesis of Linear Analog Systems

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ABSTRACT
This paper proposes a novel high level synthesis methodology for optimal linear analog systems in a formal and systematic way. It takes as an input, a high level description as well as the desired specifications of the system and gives as an output, an optimal sized architecture as well as certain constraints. This facilitates hierarchical analog system design and reduces circuit designers' effort by providing block level sizes with appropriate tolerance level. The methodology defines an abstract description of the system, selects an optimal architecture by exploring the entire architecture space and finally performs a behavioral sizing of the architecture. The entire methodology is illustrated with the case study of a state variable filter and the benefits of the approach are clearly brought out.

Categories and Subject Descriptors
B.7.2 [**Hardware**]: Integrated Circuits – *Design Aids*

General Terms:
Algorithms, Performance, Design, Verification.

Keywords
Analog High level Synthesis, Linear Systems, State Space model, Architecture exploration, L_2 Sensitivity.

1. INTRODUCTION
Analog and mixed-signal high level synthesis procedure includes the following major tasks [1]: (i) system specification (ii) architecture (system netlist) generation, (iii) performance model generation and (iv) constraints transformation.

Recently, some methods were attempted to tackle the very challenging problem of automatically generating and selecting optimal topologies. Doboli *et.al.,*[1] attempts to perform analog high level synthesis from functional specifications with an HDL based on tabu search heuristic exploration guided by the signal flow graph of the system. Symbolic performance models have been developed for the performance optimization phase. Antao *et.al.,*[2] proposed ARCHGEN, a filter synthesis tool, where architectures in controllable, observable and ladder forms are obtained from the state space description of a filter. Although the approach is systematic in comparison to the previous one, it lacks the performance optimization phase.

The main limitation of existing synthesis techniques is that most of the approaches assume the system architecture to be given and primarily focus on optimizing the parameters of the given architecture. With such restrictions on the architecture space, solutions are actually representing only local optima for a given set of requirements. Moreover, the approaches are heuristic based, putting a question about the applicability to a generic analog description and the quality of the obtained design.

In this paper, we present an original method for systematically and automatically generating optimal architecture for linear analog systems. The synthesis procedure takes as an input, a high level description of the system along with the desired specifications (performance and design constraints) and gives as an output, an optimal architecture with sizes of the architectural blocks along with the tolerance range and other constraints. These are to be passed over to the next level of design hierarchy.

Specifying the linear system in terms of algebraic description is the central paradigm of the proposed methodology. Starting from the state space description of the system, all the phases of high level synthesis, i.e., architecture generation and exploration, performance optimization, behavioral sizing and constraints translation can be constructed in a unified manner, with reasonable accuracy. Figure 1 shows the entire flow of the proposed high level synthesis flow and the various phases included within it. Operational transconductance amplifier-capacitor (OTA-C, sometimes referred to as Gm-C) based implementation style has been adopted. However, some other implementation styles like active RC or switch capacitors can easily be adopted, with minor modifications.

The paper is organized as follows. Section 2 presents the state space modeling for synthesis. Section 3 describes the performance optimization step. Architecture synthesis procedure is highlighted in Section 4. Section 5 discusses the behavioral sizing and constraint transformation. Section 6 provides experimental results. Finally, Section 7 concludes the paper.

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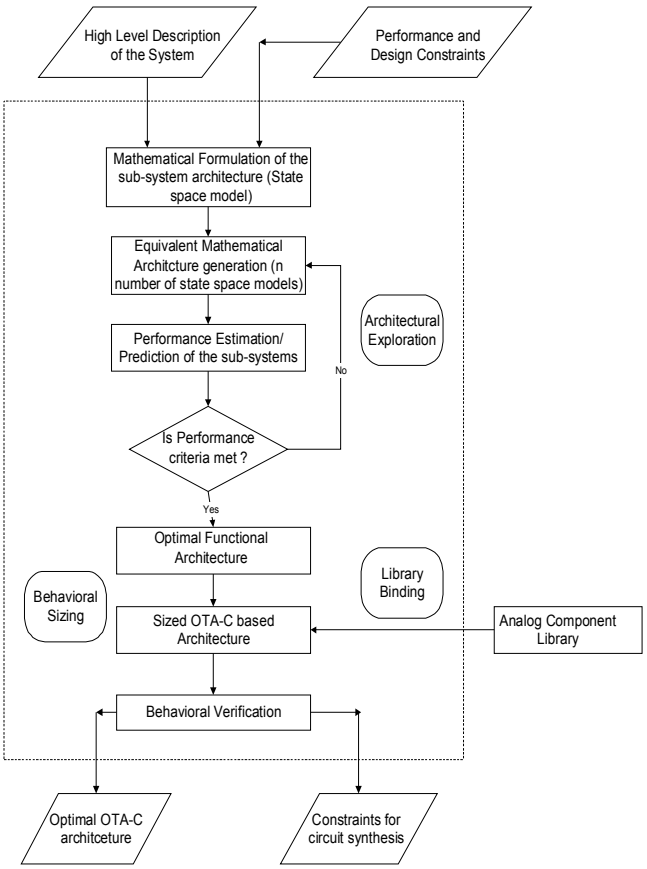

Figure 1: A Unified Flow for High Level Synthesis of Linear Analog Systems

2. STATE SPACE MODELING

In this case, since the system is a linear one, it is described by transfer function in frequency domain and state space model in time domain. Any state space model in Laplace domain (s domain) can be expressed by the following equations.

$$s\mathbf{x}(s) = \mathbf{A}\mathbf{x}(s) + \mathbf{B}\mathbf{u}(s) \quad (1a)$$

$$y(s) = \mathbf{C}\mathbf{x}(s) + Du(s) \quad (1b)$$

$\mathbf{A} \in \mathbf{R}^{nxn}$, $\mathbf{B} \in \mathbf{R}^{n}$, $\mathbf{C}^{T} \in \mathbf{R}^{n}$ and $D \in \mathbf{R}$, such that the transfer function is

$$H(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + D \quad (1c)$$

where u is the input of the system, y is the output and **x** is the state vector. **I** is the identity matrix. The number of components of the state vector **x** is equal to the order of the model (n). The state space model essentially consists of a set of input and output linear algebraic equations. Since any linear algebraic equation can easily be implemented using mathematical blocks like adders, integrators etc, these state space models encapsulate within it, all the necessary information to build linear system/sub-system architecture.

The state space models for a particular system are not unique. It can be shown that for a particular system, infinite numbers of behaviorally equivalent state space models are possible. According to the similarity transformation concept of linear system theory, if **T** be a non singular matrix, then the tuple (**A**, **B**, **C**, D) and ($\mathbf{T^{-1}AT}$,$\mathbf{T^{-1}B}$, **CT,** D) representing two different realizations are behaviorally equivalent. Therefore, once an initial state space model is specified, several different realizations are possible with suitable choice of **T** matrix. However, performance merits of the resulting architectures are not same

3. PERFORMANCE OPTIMIZATION

In analog domain, several performance figures are architecture specific. Performance metrics like power consumption, dynamic range, sensitivity of the output response to circuit component variation, etc depend upon proper selection of architectures. Architectural exploration phase explores the entire architecture space and locates a point within it, which has an optimum value of the required performance metrics. The architectural exploration loop has within itself the performance estimation phase for evaluation of these architectures. Therefore, the architectural exploration procedure serves the purpose of deciding an optimal architecture for the system and provides an initial estimation of the required specifications for each of the block.

Sensitivity of the system response to block-level component variation is an important performance metric in a hierarchical synthesis approach. This provides an indication on the manufacturability of a particular design and the faults of a circuit. This fault may occur during the hierarchically lower level of the synthesis procedure or even due to fabrication error. The L_2 norm of the sensitivity is a realistic choice of its measure. The novelty of this metric is that it provides this information at the behavioral stage of the synthesis procedure and helps to set appropriate tolerance level for the block sizes. Therefore, this metric needs to be optimized in order to make the system robust. However, fine tunings are always required at various lower level of hierarchy.

The optimization of this sensitivity metric has not been taken care of so far in any of the existing high level synthesis procedure.

3.1 Problem Formulation

The basis of our L_2 sensitivity considerations is based upon the works presented in [3,4]. The L_2 norm of the sensitivity of the transfer function to state space matrices is defined as

$$S_{L2} = tr(\mathbf{M}) + tr(\mathbf{W}) + tr(\mathbf{K}) + 1 \quad (2)$$

where **M, W** and **K** are Gramian matrices, defined as a function of the state space model. When a similarity transformation matrix is operated upon the Gramian matrices, it changes them from (**M, W, K**) to ($\mathbf{T}^{T}\mathbf{M}(\mathbf{T})\mathbf{T}$, $\mathbf{T}^{T}\mathbf{WT}$, $\mathbf{T}^{-1}\mathbf{KT}^{-T}$). Taking $\mathbf{TT}^{T}=\mathbf{P}$, the L_2 sensitivity measure in (2) is changed to

$$S_{L2}(\mathbf{P}) = tr\left[\mathbf{M}(\mathbf{P})\mathbf{P}\right] + tr(\mathbf{WP}) + tr\left(\mathbf{KP}^{-1}\right) \quad (3)$$

ignoring the insignificant unity term. Thus the problem of L_2 sensitivity minimization problem is formulated as follows.

*For a given state space model (**A**,**B**,**C**,D), determine a matrix **P**, which minimizes (3), subject to the constraint that **P** is positive definite symmetric.*

It is clear that L_2 sensitivity value changes with change in architectures, which suggests that the problem should be solved by architectural exploration method.

3.2 Solution by Architectural Exploration Method

The architectural exploration technique uses a two step procedure involving statistical global search and deterministic local search mechanisms.

Simulated annealing (SA) is used for the global search. The algorithm takes a state space model as an input and gives the estimate of an optimum state space model. The L_2 sensitivity value corresponding to the given state space serves as the initial point. In the exploration procedure, a random value of **P** matrix is chosen in the neighborhood of the current point. However, this **P** matrix needs to be positive definite symmetric.

Gradient based search technique is used in the local search procedure. The solution obtained as the output of the global procedure serves as the seed solution point for the local method. Cauchy's steepest descent method is used. The first order derivative is calculated analytically using matrix calculus formulae. The output of the local search gives a state space model which has minimum L_2 sensitivity value.

4. AUTOMATED ARCHITECTURE SYNTHESIS

The architecture synthesis procedure in the proposed approach takes place in two steps. In the first step, a functional architecture is generated from the optimal state space description. It is composed of implementation style independent functional units like adder, multiplier, integrator etc.

The second step is the synthesis of this functional architecture by replacing each of the functional units by implementation style specific realizations. The synthesis methodology uses a library of components. All system implementations only include building blocks from the library. The general structure of a voltage mode Gm-C state space system is as shown in Figure 2, the order of the system being n.

5. BEHAVIORAL SIZING AND CONSTRAINT TRANSFORMATION

The main components are operational transconductance amplifier (OTA) and capacitor (C).

The transconductance values of the structure are obtained in this step directly from the state matrix elements, available capacitor values and desired specifications.

$$Ga_{ij} = \omega a_{ij} C,\ Gb_i = \omega b_i C \text{ and } Gc_i = c_i. \quad (4)$$

Here ω is the cut-off frequency, a_{ij}, b_i and c_i are the values of the elements of the optimal state space matrices respectively. Keeping the fact in mind, that exact values of Gm can never be achievable, appropriate tolerance levels are set. This is done by varying the Gm values statistically around its nominal value and observing the output response. These Gm values along with their tolerance limits and some other constraints are the outputs of the synthesis procedure. These are to be passed to the circuit synthesis stage.

6. EXPERIMENT AND DISCUSSION

We present experiment for optimal architecture synthesis of a state variable filter and compare our results against traditional ones.

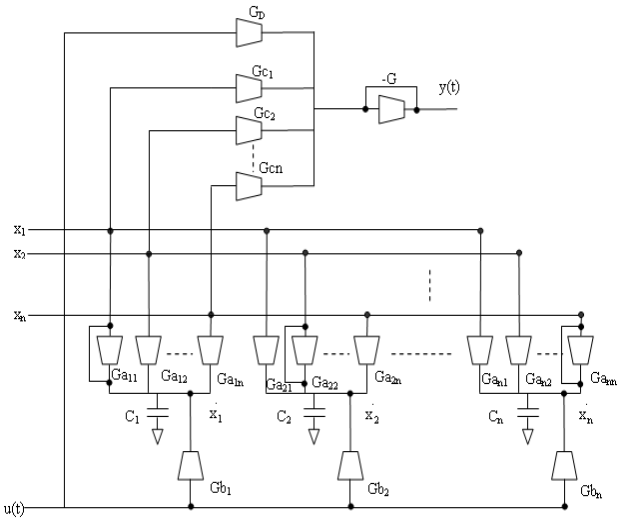

Figure 2: General Structure of a Gm-C State Space System

6.1 State Variable Filter Synthesis

The considered application is the synthesis of a higher order state variable filter. The system performances and system specifications (AC behaviour) of the filter are as follows (i) Passband Gain in between 0 dB and -2 dB (ii) Stopband gain at least -20 dB. (iii) cut off frequency = 10 Hz. (iv) Sensitivity <8 %

Based on the desired specifications, we first determine the state space model of the filter. We then generate some random invertible matrices which can be used to generate other similar state space models.

In the performance optimization phase, for moving randomly from one solution point to another, the transformation matrix **P** is chosen such that it is positive definite symmetric. With proper choice of SA parameters, the SA algorithm converges to a cost function value of 10.6540**.** The corresponding **P** matrix then serves as the seed solution point for the steepest descent local search procedure. The first derivative of the cost function is calculated analytically using matrix calculus. With the termination criteria determined by the desired sensitivity value, the algorithm converges to a cost function value of 6.4454**.**

In the automated architecture synthesis phase, the optimal state space model is first realized functionally and then by OTA-C structures. During the behavioral sizing phase, the values of the transconductances are determined using (4). We consider capacitance value of 30 pF and a capacitance multiplier gain of 50. These values are to be passed on to the circuit synthesis phase. Table 1 presents the list of few important transformed constraints. In the behavioral simulation phase, Verilog A models for all of the OTAs and capacitors are developed, and the circuit is simulated using SPICE. Figure 3 shows the gain plot obtained after the simulation. Table 2 presents the performance of the synthesized structure and compares with the desired specifications. We see a close match between the desired specifications and the synthesis results.

In order to compare the sensitivity between the optimal structure and another standard topology, we perform Monte Carlo simulations. The analysis considered a maximum of ±20% variation from the nominal value for each of the state matrix

elements, and a uniform distribution in that range for the variation. From the analysis, the optimized topology turned out to be the least sensitive one. Figure 4(a), (b) shows the simulation curve for the controllability topology and the optimized structure illustrating the sensitivity of AC response. For the controllability structure, we see that in the passband region, the curve representing the component variation differs widely from the nominal curve. However for optimized structure, in the passband region the two curves almost coincide. With this experimentation, we can set a tolerance factor of ± 20% to each Gm value. The tolerance limit is also specified in Table 1. Table 3 shows the detailed comparison result between the controllability structure and the optimized structure.

Table 1. Synthesis Output/Transformed Constraints

Parameters	Values	Tolerance
Transconductances	As calculated from (4)	± 20 %
Capacitor value	30 pF	
Capacitance multiplier	50	± 20 %
Operating Voltage	0.5*Supply Volt	
Ac amplitude Variation	100 mV	
Output Impedance	4-5 M Ω	
Load Impedance	10 pF	

Table 2. Comparison of Synthesis results with Specifications

Parameters	Specifications	Synthesis results
Passband Gain	0 dB to -2 dB	-0.2 dB
Stopband Gain	At least -20 dB	-35 dB
Cut off Frequency	10 Hz	15 Hz
Sensitivity	<8%	6.44%

Table 3. Behavioral comparison between Controllability and Optimum Structure

Parameters	Controllability	Optimum
DC Gain	-0.5dB	-0.2 dB
Cut off Frequency	13Hz	15 Hz
Trace Observability Gramian	5.3222e+07	1.4906
L_2 Sensitivity Value	5.4806e+07	6.4454

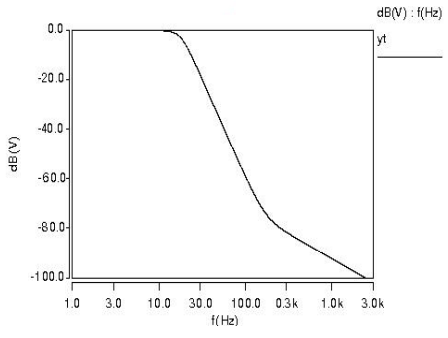

Figure 3: SPICE simulated Bode Plot of the Synthesized Structure

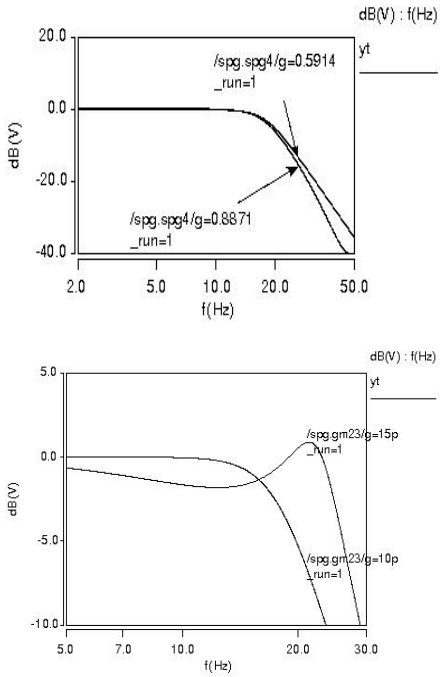

Figure 4(a): Monte Carlo plot for the optimized structure and (b) Controllability structure

7. CONCLUSION

A novel way of synthesizing optimal linear analog system in a formal and systematic way has been presented. Synthesis results are architectures of sized OTAs and capacitors with appropriate tolerances and some specific constraints such that the desired performance specifications are satisfied. In particular, this technique has been shown to be able to minimize the L_2 sensitivity of the target system that is supposed to be a vital performance metric. The feasibility of the method has been demonstrated by the synthesis of a state space filter. Behavioral simulation results of the system architecture closely matches with the desired specifications. The synthesized architecture has been compared with traditional ones in terms of the optimization criterion.

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