High Level Synthesis of Higher Order Continuous Time State Variable Filters with Minimum Sensitivity and Hardware Count

Soumya Pandit Sougata Kar* Chittaranjan Mandal Amit Patra
*Indian Institute of Technology, Kharagpur, India *Jadavpur University, India*
E-Mail: soumya_pandit@ieee.org

Abstract

The sensitivity of the response of an analog system to circuit parameter variations is a vital performance metric for evaluation of its quality. This paper proposes a unified high level synthesis methodology for higher order continuous time state variable filters, considering the optimization of this metric. Minimization of the hardware count, which is another important issue, has also been taken into account at a much earlier stage of design. The entire methodology is illustrated with the case study of a state variable low pass filter and the benefits of the approach are clearly brought out.

1. Introduction

This paper is one of the few attempts to present a unified synthesis environment for higher order continuous time state variable filters considering the minimization of the sensitivity of system response to circuit component variation and hardware count. In contrast to the existing approaches [1], the methodology is formal and systematic. Also, it is generic enough to accommodate the synthesis of any arbitrary linear analog systems.

2. High Level Synthesis of Analog State Variable Filter

Since the system is a linear one, it is described by state space model in time domain, given by the matrix tuple (**A**, **B**, **C**, D) [2]. For architecture generation, the system functionality is described as signal flow and processing. State space models can be synthesized into behavioral block architectures (BBAs) using analog computation model. The architectural exploration is based on the concept of 'similarity transformation' [2]. According to this concept two different state space models related by this transformation are identical in input-output characteristics, but may differ in terms of a given performance measure. Thus, a major task of the synthesis

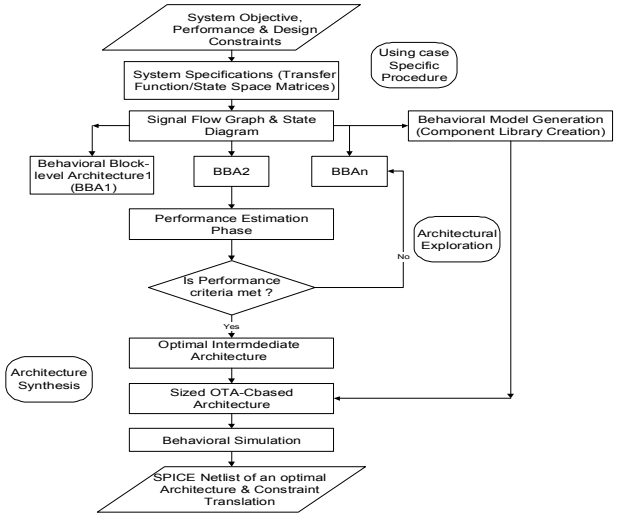

Figure 1: Framework for High level Synthesis

procedure is to select an architecture so that system-level design objectives are satisfied and certain performance constraints are optimized. The framework is illustrated in Figure 1.

3. Performance Optimization

This phase evaluates the quality of BBAs. Sensitivity of the architecture output to circuit parameter variations is a vital performance metric, providing an indication on the manufacturability of a particular design. An expression for L_2 norm measure of the sensitivity is as follows. The detailed derivation is given in the internal report [3]. Equation (1) serves as the cost function.

$$S_{L2}(\mathbf{P}) = tr\left[\frac{1}{2\pi}\int_0^{2\pi}\mathbf{P}\mathbf{N}\left(e^{j\omega}\right)\mathbf{P}^{-1}\mathbf{N}^T\left(e^{-j\omega}\right)d\omega\right] + tr(\mathbf{P}\mathbf{W}) + tr\left(\mathbf{P}^{-1}\mathbf{K}\right) \quad (1)$$

In the above equation tr[**X**] means the trace of the matrix **X.** **N**, **W**, and **K** represent three Gramian matrices respectively. **W** and **K** are referred to as observability

Gramian matrix and controllability Gramian matrix respectively in deterministic control system theory [2]. All the three Gramians are functions of the state space matrices **A**, **B**, and **C**. The matrix **P** is positive-definite symmetric and $\mathbf{P=TT^T}$, **T** is the similarity transformation matrix, characterizing the architectural exploration.

The minimization problem is therefore to obtain a state space model for which this sensitivity measure is minimum. The optimization strategy we use is a numerical one, employing both local and global methods.

One practical disadvantage with the resulting optimal model is that all the state space matrices are found to be dense. This means that the number of circuit components required to implement the model is large. In order to reduce the hardware count, as many zeros as possible should be introduced within the optimal state space matrices. However, with this introduction, the value of L_2 sensitivity must not be changed. This is achieved by applying orthogonal similarity transformation on the model so that the densest **A** matrix is converted to its Hesseberg form [4]. Sparse state space models can be synthesized with reduced number of circuit components.

4. Case Study

In order to illustrate the steps of the synthesis procedure discussed above, a case study is considered where we synthesize a low pass state variable filter with minimum sensitivity and hardware count. For space limitations, we present only the SPICE simulation results (see Table 1) of the synthesized OTA-C architecture and the Monte Carlo simulation plots for sensitivity analysis (see Figure 2(a), 2(b)). More details can be found in [3].

Table 1: Synthesis Results

	Parameters	Specifications	Synthesis Results
1	Order	4	4
2	Transfer Function	H (s)	H(s)
3	Passband gain	Between 0db to -2 dB	- 0.2 dB
4	Stopband gain	At least - 20 dB	-35 dB
5	Cut off frequency	10 Hz	15 Hz
6	Minimum L_2 sensitivity	x	6.447, **P**
7	Optimal State Space	x	**A**, **B**, **C**,D

$$\mathbf{P}=\begin{bmatrix} 41.8039 & -21.9053 & 9.1875 & -3.2732 \\ -21.9053 & 18.7604 & -8.2827 & 4.9107 \\ 9.1875 & -8.2827 & 12.8459 & -5.0437 \\ -3.2732 & 4.9107 & -5.0437 & 8.2529 \end{bmatrix} \quad \mathbf{A}=\begin{bmatrix} -12.38 & 2.309 & 0.9079 & -1.053 \\ -11.27 & -8.442 & -3.152 & 0.9342 \\ 0 & 11.97 & -5.667 & 6.07 \\ 0 & 0 & -11.35 & -2.936 \end{bmatrix}$$

$$\mathbf{B}=\begin{bmatrix} 2.434 \\ -1.506 \\ -0.282 \\ -0.06036 \end{bmatrix} \quad \mathbf{C}=\begin{bmatrix} -0.1538 \\ -0.5914 \\ 1.299 \\ 2.489 \end{bmatrix}^T \quad D=0$$

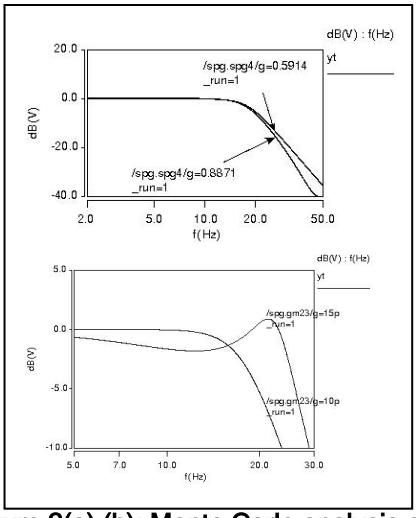

Figure 2(a) (b): Monte Carlo analysis of Synthesized and another un-optimized (controllability) structure.

From table 1 and simulation curves, it is evident that there is a close match between the synthesized results and the desired specifications. The slight discrepancies can easily be handled during circuit synthesis. Moreover, the synthesized architecture is more robust compared to other generated structures.

5. Conclusion

This paper presents an efficient methodology for high level synthesis of higher order analog state variable filters. The framework is designed to be generic enough to accommodate the synthesis of any arbitrary linear analog systems. The sensitivity of the filter response to circuit component variation is optimized. Redundant hardware components are removed without affecting either the terminal characteristics or sensitivity value. The feasibility of the method has been demonstrated by taking a case study for the synthesis of low pass state variable filter. Numerical results validate the procedure. The main benefit of the presented high level synthesis methodology is that it allows the design of robust linear analog circuits at a low cost and in short time without having an in-depth knowledge of analog circuit design.

6. References

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