High Level Synthesis of Linear Analog Systems

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Abstract*—This paper presents a unified framework for high level synthesis of linear analog systems, which is now an important research area in analog VLSI systems design. The salient features of this synthesis methodology are automated synthesis of system architectures and performance optimization by architectural exploration method. Operational transconductance amplifier (OTA) and capacitor (C) based implementation style has been adopted for the synthesis step. The entire framework is illustrated with the case study of a low pass filter and the benefits of the approach are clearly brought out.

I. INTRODUCTION

The key to manage the increased design complexity of today's VLSI systems, while meeting the shortening time-to-market factor, is the use of computer-aided-design (CAD) and verification tools. Although, well established CAD tools are there in digital domain, no standardized CAD tool exists so far for analog system design, which completely automates the analog design flow. The major reason behind this lack of automation tool is due to the inherent difficulties involved within the problem itself. Analog design, in general is perceived as less systematic and more heuristic and knowledge-intensive in nature. A typical CAD flow for analog system design consists of three main parts --- (i) high level synthesis (system synthesis) and verification, (ii) circuit synthesis and verification and (iii) layout synthesis and verification

In this paper we propose a unified framework for the high level synthesis of linear analog systems. The presented methodology takes the design specifications and performance constraints as input and generates the SPICE netlist of an architecture, which satisfies the design specifications and performance constraints. Unlike the existing approaches [1 and references cited there], the proposed methodology is systematic and has the potentiality of synthesizing architectures, optimized for almost all important system level performance criteria like ac performance, sensitivity, dynamic range, power consumption etc. Although in this paper, for brevity purpose, we will consider only the minimization of the sensitivity of system response to component variation.

The paper is organized as follows. Section II gives a detail overview of the proposed high level synthesis methodology. Section III discusses the architecture synthesis mechanism and performance optimization phase. Section IV presents a case study along with the behavioral simulation results and finally, section V concludes the paper.

II. HIGH LEVEL SYNTHESIS METHODOLOGY

The proposed flow for high level synthesis of linear analog systems is shown in the figure 1. System specifications provide an abstract description of the system and the signal flow within it without illustrating details on the hardware realization. Since the targeted system is a linear one, it may be described by transfer function in frequency domain and state space model in time domain. The state space model is of the form shown below

$$s\mathbf{x}(s) = \mathbf{A}\mathbf{x}(s) + \mathbf{B}u(s) \quad (1)$$

$$y(s) = \mathbf{C}\mathbf{x}(s) + Du(s) \quad (2)$$

such that the transfer function is as follows.

$$H(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + D \quad (3)$$

where **I** is an identity matrix, u is the input of the system, y is the output and **x** is the state vector. The number of components of the state vector **x** is equal to the order of the model. (**A**,**B**,**C**,D) are the state space matrices.

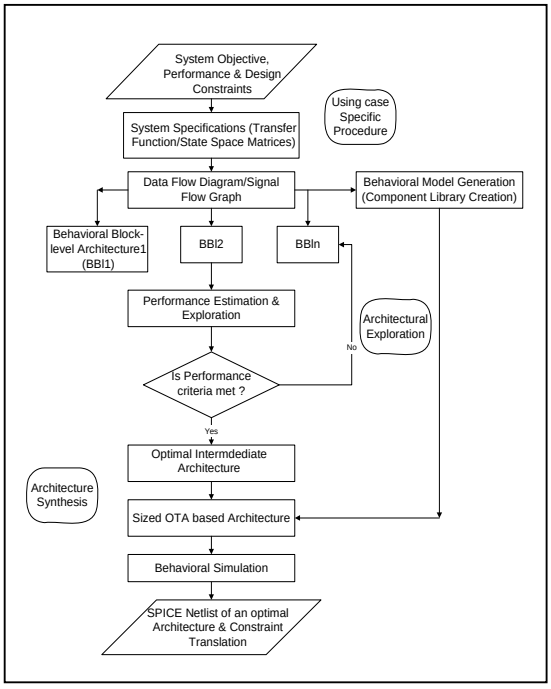

Figure 1. Flow for High Level Synthesis of Linear Analog Systems

Using analog computation model, a behavioral block level architecture can be constructed from the state space model, in terms of signal processing blocks like integrators, adders and scalar multipliers. Generating alternative behavioral block level architectures from one state space model are possible using the similarity transformation concept. According to this concept, if **T** be a non singular matrix, then the tuple (**A, B**, **C**, D) and ($\mathbf{T}^{-1}\mathbf{AT}$,$\mathbf{T}^{-1}\mathbf{B}$, **CT**, **D**) representing two different realizations are behaviorally equivalent.

The implementation style is chosen to be based upon operational transconductance amplifier (OTA)-capacitor (C) structure [2]. The choice is motivated by the fact that OTA-C structures offer advantages in terms of design simplicity, high frequency capability, electronic tunability, monolithic integrability and reduced component count. However, the methodology is equally applicable for other implementation styles like active RC, switch capacitors etc with some obvious modifications. The performance optimization module takes the state space representation of the behavioral architectures as input. Certain performance metrics are estimated for all of these intermediate architectures and an optimal one is chosen. Optimizing the AC behaviour is not mandatory in our approach, because all the architectures have identical terminal characteristics which ensure that all of them will meet the desired AC characteristics. Once an optimal architecture is chosen, the mathematical blocks in the synthesized architecture are replaced by appropriate behavioral models chosen from the library. The behavioral simulation phase verifies the performance of the synthesized architecture against the design specifications and performance constraints.

III. ARCHITECTURE SYNTHESIS AND PERFORMANCE OPTIMIZATION

A. OTA-C based Architecture Synthesis

The synthesis methodology uses the state space formulation to realize higher order transfer function using multiple loop feedback approach. We assume canonical realization of state space model. This will reduce volume, noise, parasitic effects and power dissipation. Also we consider grounded capacitors only, which can absorb parasitic capacitances and need smaller cheap area than floating ones.

The general structure of voltage mode state space OTA-C system is shown in figure 2. An analytical description of the circuit in Laplace domain is given by the following matrix equations,

$$\begin{bmatrix} sC_1 - G_{a11} & & \\ & \ddots & \\ & & sC_n - G_{ann} \end{bmatrix} \begin{bmatrix} x_1 \\ \vdots \\ x_n \end{bmatrix} = \begin{bmatrix} 0 & \cdots & G_{a1n} \\ \vdots & \ddots & \vdots \\ G_{an1} & \cdots & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ \vdots \\ x_n \end{bmatrix} + \begin{bmatrix} G_{b1} \\ \vdots \\ G_{bn} \end{bmatrix} u(s) \tag{4}$$

$$y(s) = \begin{bmatrix} G_{c1} & \cdots & G_{cn} \end{bmatrix} \begin{bmatrix} x_1 \\ \vdots \\ x_n \end{bmatrix} + G_D u(s) \tag{5}$$

The voltage at the ith node x_i is denoted by x_i. Equations (4) and (5) can be written in compact notation as follows.

$$\mathbf{Y}\mathbf{x}(s) = \mathbf{G}_a\mathbf{x}(s) + \mathbf{G}_b u(s) \tag{6}$$

$$\mathrm{y}(s) = \mathbf{G}_c\mathbf{x}(s) + G_D u(s) \tag{7}$$

From (6) and (7), we can calculate the transfer function of the generic Gm-C state space filter. It is given as follows.

$$H_G(s) = \mathbf{G}_c\left(\mathbf{Y} - \mathbf{G}_a\right)^{-1}\mathbf{G}_b + G_D \tag{8}$$

It is to be noted that the transfer function as expressed in (8) has the dimension of conductance. To make it dimensionless, we need to multiply it by impedance, which is achieved by the transconductance simulated resistance at the output (see fig 2).

Since we are considering single output OTA structure with canonical realization, with the number of OTAs determined by the elements of the state space matrices, a way to reduce the number of OTAs is to introduce as much zeros as possible within the matrices, without altering its performance characteristics [3]. An important tool to create zeros in a vector is to multiply the vector by a Householder matrix [4].

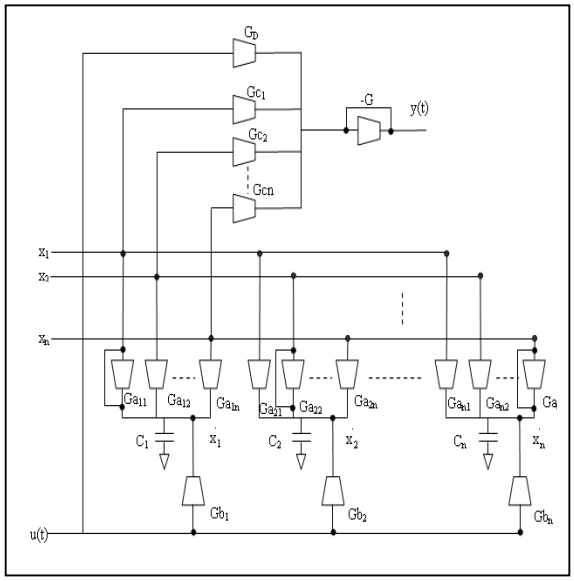

Figure 2. Generic structure of a voltage mode Gm-C state space system.

With this a real arbitrary matrix can be reduced to Hessenberg form. Since the Householder transformation is basically an orthogonal similarity transformation, the behavioral properties of the state space remains unchanged, when operated by it.

B. Performance Optimization

Sensitivity to circuit parameter variations is a vital performance metric, providing an indication on the manufacturability of a particular design. Moreover, introduction of any unwanted entities like parasitics, noise etc may lead to deviation in the elements of state space matrix from its typical value. The L_2 norm of the sensitivity [5] matrix is a realistic choice of its measure. An expression for L_2 sensitivity is given below [3]. It serves as our cost function that is to be minimized.

$$S_{L2}(\mathbf{P}) = tr\left[\frac{1}{2\pi}\int_0^{2\pi}\mathbf{PN}\left(e^{j\omega}\right)\mathbf{P}^{-1}\mathbf{N}^T\left(e^{-j\omega}\right)d\omega\right] + tr\left(\mathbf{PW}\right) + tr\left(\mathbf{P}^{-1}\mathbf{K}\right) \quad (9)$$

In the above expression tr[**X**] means the trace of the matrix **X,** **N**, **W**, and **K** represent three Gramian matrices respectively. **W** and **K** are referred to as observability Gramian matrix and controllability Gramian matrix respectively in deterministic control system theory. All the three Gramians are functions of the state space matrices **A**, **B**, and **C**. The matrix **P** is positive-definite symmetric and $\mathbf{P=TT}^T$**,** **T** is similarity transformation matrix.

The exploration strategy, we use is a two step procedure employing both local and global approaches. For global search, we use simulated annealing. Since **P** is dependent upon **A**, **B**, and **C**, the global procedure calculates the value of S_{L2}(**P**) for numerous (**A**,**B**,**C**). The minimum valued realization obtained in the first step serves as the initial point for the second step of optimization. We use gradient based search technique for local optimization procedure. In this step an optimum value of (**A**,**B**,**C**,D) is obtained. While choosing the next solution from the current point, constraints are to be imposed so that the **P** matrix is positive definite symmetric, and the similarity transformation matrix **T** is non-singular.

IV. CASE STUDY

The application used to illustrate the methodology is the synthesis of a Butterworth filter. The given design specifications are as follows. (i) Passband gain to lie between 1 and Gp = 0.794 (-2dB) for $0 \le \omega < 10$. (ii) Stopband gain not to exceed Gs = 0.1(-20dB) for $\omega \ge 20$. The filter must have minimum sensitivity to component variation.

From the given specifications, we generate the order, transfer function and the state space model using Matlab. Several state space models can be generated using similarity transformations. The performance estimation and exploration phase selects an intermediate architecture, which has the minimum L_2 sensitivity. Using suitable Householder transformations, zeros are introduced in the state matrix such that the value of L_2 sensitivity is not altered. The resulting architecture, given by the tuple (**A**opt, **B**opt**,** **C**opt**,** Dopt) is then synthesized. The synthesis results are tabulated in table 1 and the corresponding OTA architecture is shown in fig 3. The values of the transconductances are determined as $Ga_{ij} = \omega a_{ij}C$, $Gb_i = \omega b_i C$ and $Gc_i = c_i$. Here ω is the cut-off frequency, a_{ij}, b_i and c_i are the values of the elements of the **A**opt, **B**opt, **C**opt state space matrices respectively The design is verified against the specifications. The synthesized Bode plot is shown in fig 4. From table 1, we see that there is a close match between the desired specifications and the synthesis results.

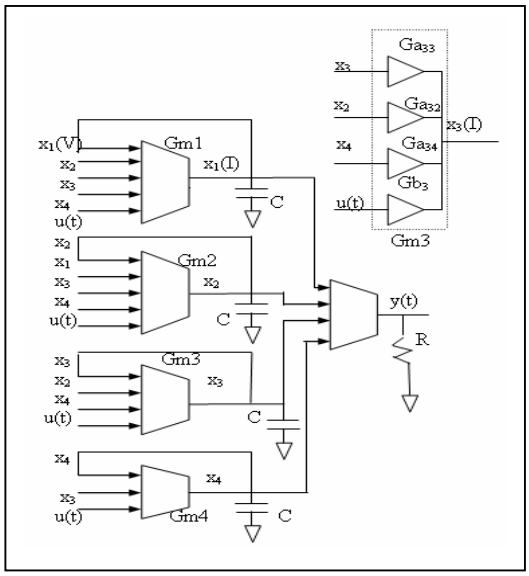

Figure 3. OTA-C implementation of optimized filter

TABLE I. COMPARISON BETWEEN SPECIFICATIONS & SYNTHESIS RESULTS

Parameters	Specifications	Synthesis Results
Order	4	4
Passband gain	Between 0dB and -2 dB	- 0.2 dB
Stopband gain	At least -20dB	-35dB
Cut off frequency	10 Hz	15 Hz
Minimum L_2 sensitivity	x	6.447
Optimal State Space	x	(**A**opt, **B**opt, **C**opt**,** Dopt)

$$\mathbf{A}\text{opt} = \begin{bmatrix} -12.38 & 2.309 & 0.9079 & -1.053 \\ -11.27 & -8.442 & -3.152 & 0.9342 \\ 0 & 11.97 & -5.667 & 6.07 \\ 0 & 0 & -11.35 & -2.936 \end{bmatrix} \quad \mathbf{B}\text{opt} = \begin{bmatrix} 2.434 \\ -1.506 \\ -0.282 \\ -0.06036 \end{bmatrix}$$

$$\mathbf{C}\text{opt} = \begin{bmatrix} -0.1538 & -0.5914 & 1.299 & 2.489 \end{bmatrix} \qquad \text{Dopt} = 0$$

For comparing the sensitivity of the resulting structure and an unoptimized (controllability) structure, we perform Monte Carlo analysis. The curves are shown in fig 5(a) and 5(b). It is seen that the optimized structure outperforms the controllability structure in the region of interest.

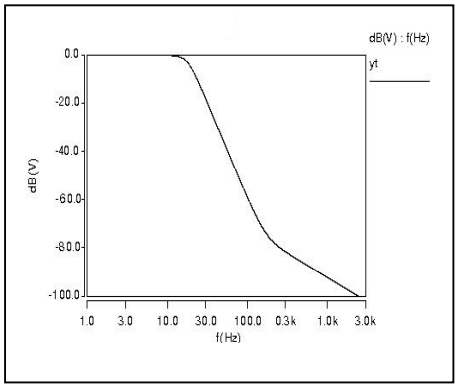

Figure 4. Synthesized Bode Plot.

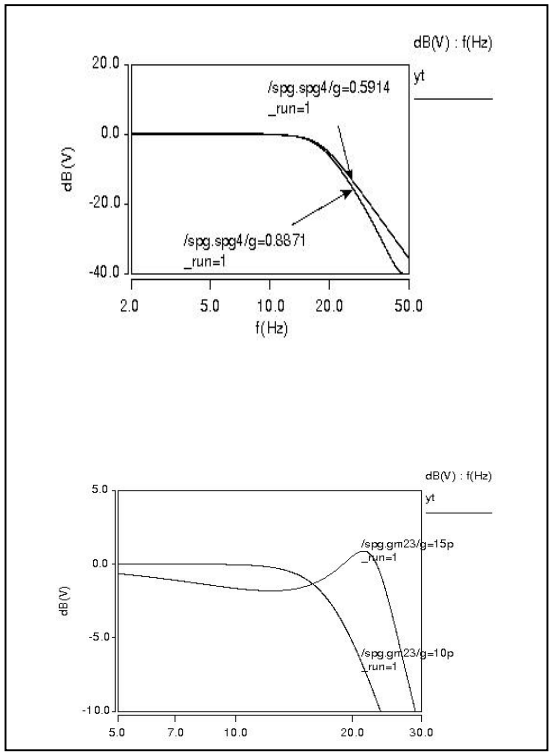

Figure 5(a) & (b). Monte Carlo analysis plot for the optimized and unoptimized structure.

V. CONCLUSION

A formal and systematic approach for high level synthesis of linear analog systems, which is considered as an important emerging area in CAD for VLSI design, has been presented. This synthesis methodology incorporates architecture exploration and optimization with respect to given performance metrics. In particular, this technique has been shown to be able to minimize the L_2 sensitivity of the target system. OTA-C based implementation style has been adopted for the synthesis step. The feasibility of the method has been demonstrated by the synthesis of a 4^{th} order low pass filter.

VI. REFERENCES

[1]. Doboli, A. and Vemuri, R., Exploration-Based High-Level Synthesis of Linear Analog Systems Operating at Low/Medium Frequencies. IEEE Trans. CADICS, vol. 22, no 11, Nov 2003, pp., 1556-1567

[2]. Ray., B.N., Chaudhuri P.P., & Nandi P.K., Efficient Synthesis of OTA Network for Linear Analog Functions. IEEE Trans. CADICS, vol 21., No 6, May 2002 pp517-533.

[3]. Pandit,S. High Level Synthesis of Higher Order Continuous Time State Variable Filter with Minimum Sensitivity and Hardware Count, Accepted for publications at DATE 2006

[4]. Strang. G., Linear Algebra and its Applications. 3rd Edition Harcourt Brace Jovanovich, Publishers 1988

[5]. Hinamoto, T., Iwata,K., and Lu, W.S., State Space Digital Filters with Minimum L_2 Sensitivity subject to L_2 scaling constraints. Proc., ICASSP'05, vol 4. March 2005, pp., IV-265 - IV-268