CS60089 TESTING AND VERIFICATION OF CIRCUITS L-T-P: 3-1-0, Credit: 4

Course Instructors: Pallab Dasgupta & Rolf Drechsler

The course Testing and Verification of Circuits is often misconceived by the students as heavily biased towards circuit design practices. This is not true. Modern techniques for verification and testing of circuits deals with advanced automata, symbolic representations of large state spaces, algorithms, advanced logic and deduction. This is a course meant for students having adequate background in formal languages and automata theory, logic design, and algorithms.

The core outline of the course is given below. I am also pleased to announce that a module of six lectures in this course will be offered by Prof Rolf Drechsler of the Technical University of Bremen, Germany. The outline of his module is also given below. Professor Drechsler is one of the leading experts in this technology and he brings with him many years of advanced research conducted by him and his research group.

Course Outline

- Introduction
- Symbolic representations of combinational logic and finite state machines (BDD, SAT)
- Symbolic reachability of large state spaces
- Simulation Techniques
- Fault simulation
- Test generation for combinational circuits
- Formal Equivalence checking
- Temporal Logic and Assertions
- Automata over infinite words
- Model Checking
- Sequential ATPG
- Advanced topics: Verification/Testing of Analog circuits
- Hybrid System Analysis

Lectures by Prof. Rolf Drechsler "Advanced Formal Techniques along the Design Flow"

- Motivation
- Proof techniques
  - Boolean(DDs, satisfiability) , word-level (extensions of DD, SMT solvers)
- Verification
  - Simulation vs. formal, constrained random simulation, measuring coverage
- Debugging
  - Finding faults, error assumptions, corrections
- Test
  - Black box vs. white box, encoding, hybrid approaches
- Conclusions

Reference Books

Testing

1. N. K. Jha and S. Gupta, Testing of Digital Systems, Cambridge University Press.
2. M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing, Kluwer Academic Publishers.

Verification

3. Gary D. Hachtel and Fabio Somenzi, Logic Synthesis and Verification Algorithms
4. Thomas Kropf, Introduction to Formal Hardware Verification
5. Pallab Dasgupta, A Roadmap for Formal Property Verification
6. Christel Baier and Joost-Pieter Katoen, Principles of Model Checking
7. Rolf Drechsler, Formal Verification of Circuits, Springer
8. Rolf Drechsler and R Ebendt and G Fey, Advanced BDD Optimization, Springer