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Micro-controller for Sensor Networks

Design of a micro-controller geared toward sensor network applications

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Section A: INTRODUCTION

A sensor network is a term referring, in general, to a collection of networked embedded systems. Each of the systems constituting the network is called a sensor node or just a node [1].

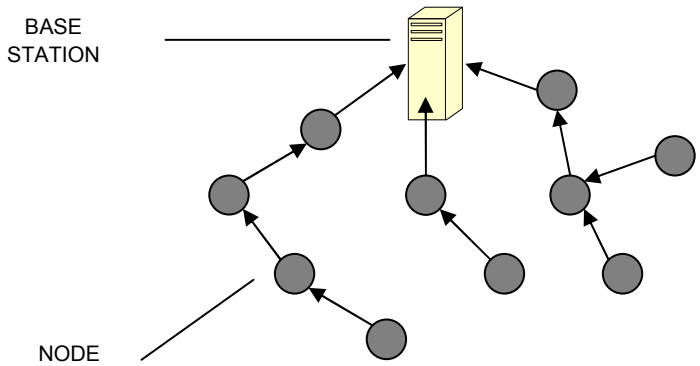


Fig. A SENSOR NETWORK

Each sensor node has the following basic functions:

- **Data Sampling**
  - Gather data from the environment.
- **Data Processing**
  - Process the data using the node's processing capabilities.
- **Data Communication**
  - Relay data to other nodes through the network.

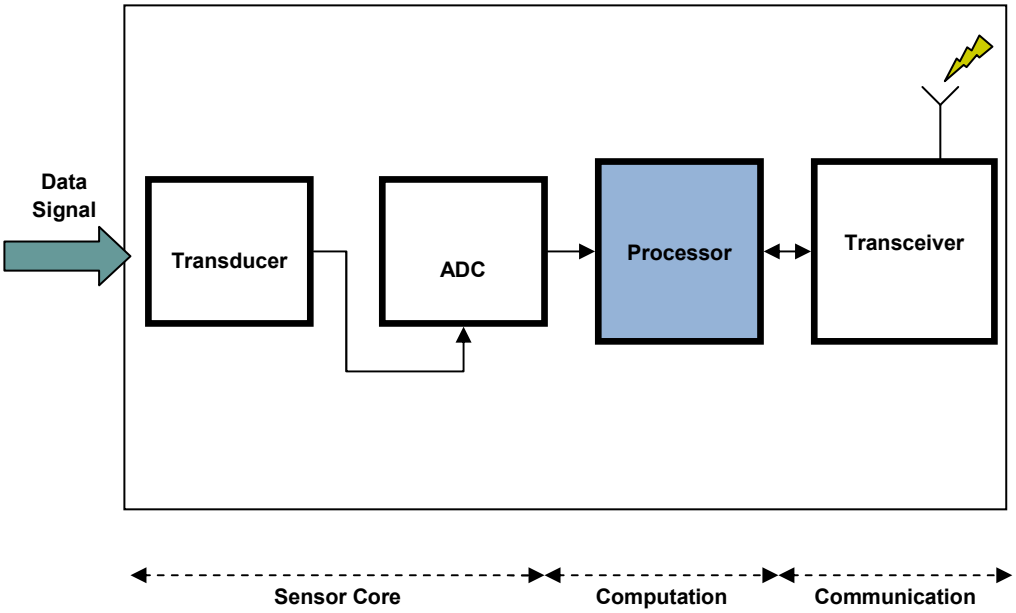


Fig. BASIC ARCHITECTURE OF A SENSOR NODE

Although computer-based instrumentation has existed for a long time, the density of instrumentation made possible by a shift to mass-produced intelligent sensors and the use of pervasive networking technology gives sensor networks a new kind of scope that can be applied to a wide range of uses. These can be roughly differentiated into:

- **Monitoring space**
    - Environmental monitoring.
    - Precision Agriculture.
    - Alarm and Security Systems.
    - Climate control and surveillance.
- **Monitoring objects**
    - Structural monitoring.
    - Motion detection.
    - Healthcare.
    - Automated Manufacturing.
- **Monitoring the interactions of objects with each other**
    - Wildlife monitoring.
    - Homeland security.

Sensor nodes can use many communication media to relay information through the network, but there is an increasing trend towards the medium being wireless because for large networks, laying cables is a daunting task [2]. Thus, wireless sensors networks (WSNs) are becoming increasingly popular over wired sensor networks.

In this project we actually look at the processor part of a sensor node. Our basic objective is to propose an architecture that is better suited to sensor network applications than commonly available off-the-shelf micro-controllers [3] that are currently in use..

Section B: MOTIVATION

In their survey of processor choices for sensor networks [3], Lynch and O' Reilly show us a handful of commercial processors that can be used today for sensor network applications. The paper shows a wide disparity in the features and instruction sets of these processors. It concludes by saying that the MSP430 is the better suited of the current commercial processors.

The paper clearly shows the paucity of processors specifically targeted towards the sensor network domain, rather all the processors in use by sensor network deployment are general RISC processors that target a large variety of embedded systems. This in-turn causes their designs to be laced with too many generalities as can be seen from the wide variety and disparity of different processor's features explored in [2] and [3]. These generalities in-effect make the design inefficient for specific sensor network applications. Generally, these processors have hardware which is not required by the sensor node at all and just wastes power.

We instead try to take a different approach to processor design and attempt to come up with a micro-controller tailored to the common application needs of the sensor network domain, while stripping off useless features to increase efficiency.

There have been other forays into this area like the SNAP/LE [4]. The only problem with these designs is that they are asynchronous and remain theoretical with no hardware simulation or actual fabrication data is available to support their claims. These designs are promising but still in the future.

We instead will follow a conventional synchronous design, not with the view of proposing a new design idea or paradigm but with the view of making conventional designs more tailored to sensor network applications. This approach will also give us the opportunity to fabricate and conduct hardware simulation of our design.

To recapitulate, our motivations for this ASIC design are:

- Dearth of sensor network specific processors.
- The remaining designs are theoretical and fabrication is way in the future due to use of unconventional design techniques.
- Paucity of actual fabrication or hardware simulation of the processor design.

Section C: DESIGN BACKGROUND

This section explores the various requirements and issues of general sensor node processors/ controllers. Studies of the basic features required by common sensor network applications are explored to give us a background for our design.

Sensor network processors introduce an unprecedented level of compact and portable computing. These small processing systems reside in the environment which they monitor, combining sensing, computation, storage, communication, and power supplies into small form factors. Sensor processors have a wide variety of applications in medical monitoring, environmental sensing, industrial inspection, and military surveillance. Despite efforts to design suitable processors for these systems [4], there is no well-defined method to evaluate their performance and energy consumption. The historically used MIPS (millions of instructions per second) and EPI (energy per instruction) metrics cannot provide an accurate comparison because of their dependence on the nature of instructions, which differ across instruction set architectures.

To properly evaluate architectures and get an idea of the kind of benchmark algorithms we must gear our design towards, we use the ideas on WiSeNBench [8] and SenseBench [9]. These benchmarks help us come with a basic level of requirements to help in design of our processor. This, along with a survey of commonly used features of current sensor network micro-controllers, like the MSP430 [7] and ATMega128 [6], in sensor network applications forms the basis for our design features.

We use conventional low-power micro-controller design techniques suited to the features which best fit the sensor network applications. This will help us come up with efficient, easily usable micro-controller that can be manufactured using the current fabrication technology.

The main findings from the test-benches, benchmarks and literature are summarized as follows:

- Power is the key objective in sensor network processors i.e. low-power modes are useful.
- RISC-based processors work best as complicated instructions like multiplication and DSP abilities are rarely required by sensor nodes applications which are meant to be lightweight [8].
- Sensor nodes are typically interrupting driven systems and so need a good interrupt structure.
- The SenseBench and WiSeNBench use the following basic sensor network algorithms:
    - Crypto / Security:
        - CRC, Hash Algorithms, MD5, RC6

- Basic Core Algorithms:
  - Sorting, Fibonacci, Binary Search, Min-max finder, Sum-array, Majority, Top10
- Compression:
  - RLE (run-length encoding) ,Wavelet encoding
- Basic communication algorithms:
  - Routing (SMAC, routing)
  - Radio (encoding etc.)

- Results for the test-bench algorithms for common architectures (8-bit coolRISC, PIC8, PIC16, MSP430 and ATMega128):
  - Code size
    - Most algorithms have code sizes under 500 bytes for 16-bit architectures.
    - For the 8-bit RISC architectures, size was under 700 bytes.
  - Memory access
    - All algorithms have 40 to 60% instructions as memory accesses for both the 8-bit and 16-bit architectures.
  - Frequent instructions
    - Load, Store, Add, Sub, R-shift, L-Shift, Mov, Xor. All other instructions occur less than 1% of the time.
- I/O Requirements:
  - Most data generating phenomena have the following requirements:

Phenomenon	Sampling (Hz)	Resolution (bits)
Atmospheric temperature	0.017 - 1	8
Barometric pressure	0.017 - 1	8
Body temperature	0.1 - 1	8
Seismic vibration	0.2 - 100	8 - 12
Blood pressure	50 - 100	8 - 10
Engine temp / pressure	100 - 150	8 - 10
ECG (electro-cardiogram)	100 - 250	8 - 16

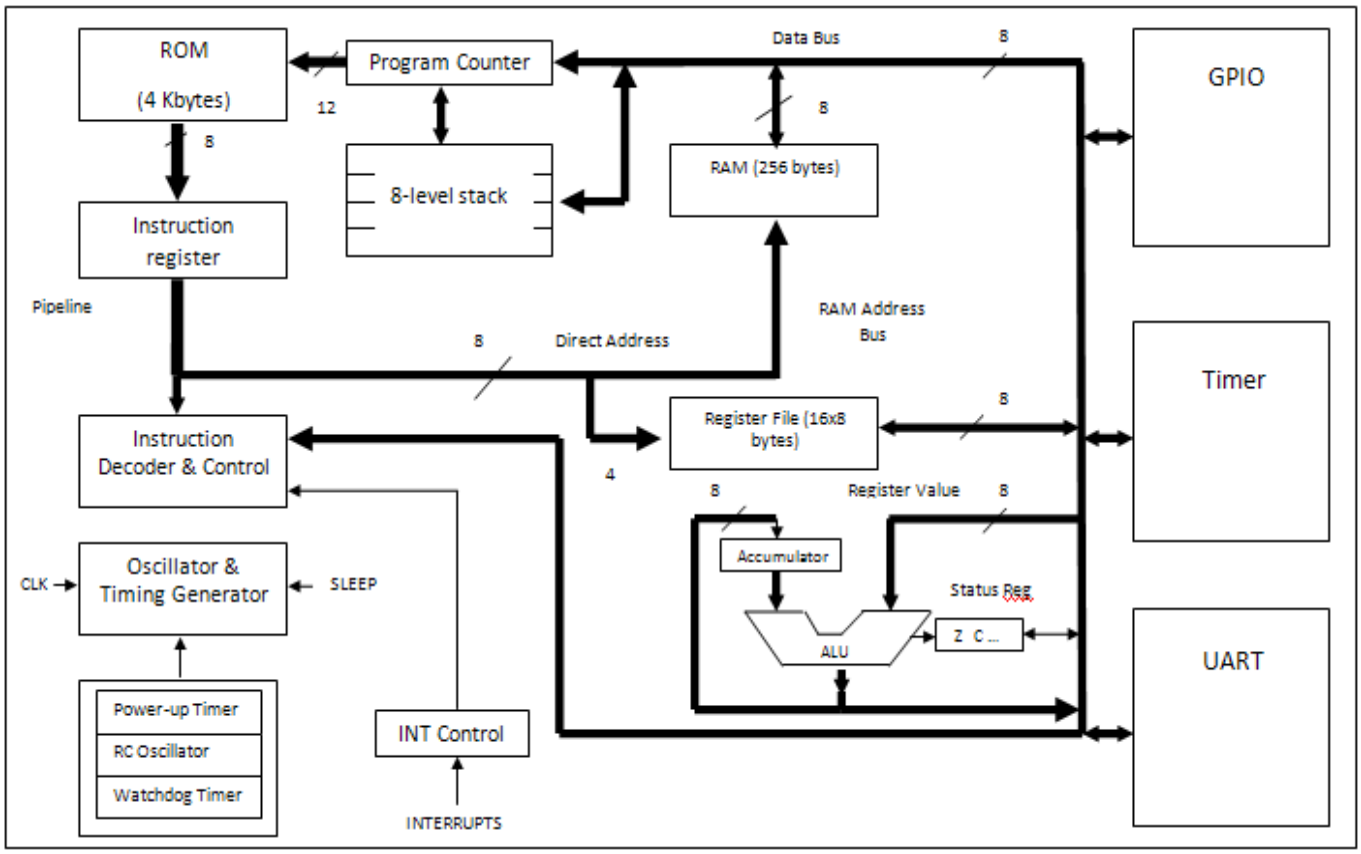
The above requirement guidelines along with the literature survey of common coolRISC [10], MSP430 [7], ATMega128 [6] and PIC [5] series of micro-controllers help us propose our final architecture, instruction set and basic I/O features.

Section D: THE ARCHITECTURE

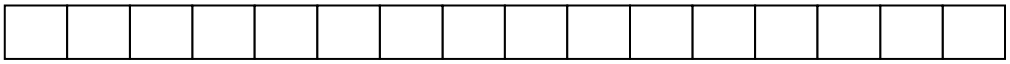
Using the requirement guidelines we give a summary of the proposed architecture and instruction-set in this section. Simulation details and comparison with other processors will follow in the complete dissertation.

Architectural Features

- 8-bit synchronous RISC-based processor with Harvard memory architecture
  - Data Memory: 256 Bytes (SRAM).
  - Program Memory: 4 KB (Flash).
  - Load-Store RISC based with 1 or 2 byte instructions.
  - 16 X 8-bit GPRs
  - Stack for fast context-switching: 8 levels
- **Pipelining**: two-stage pipeline with Fetch-Execute.
- **I/O Features**: 1 GPIO (8 bit), UART (for PC interfacing).
- **Interrupt Structure**: Two general purpose interrupts with priority levels and mask-able.
- **Timers**: Watchdog and 16-bit timer.
- **Two Sleep Modes**: Low-frequency "clock swap" and non-essential features' shut off.



Instruction Set Architecture



BIT NO.

ADD, SUB	Register Address

Arithmetic Operations

AND, OR, XOR	Register Address

And, Or, Xor & Not Boolean operations

LSHIFT, RSHIFT

Standard bit left or right shift

MOV TO/FROM	Register Address

Register Move to/from Acc

INT_CONTROL

Interrupt priority/mask operations

LOAD, STORE	Data Memory Address

RAM Operations

CONST	8-bit Constant

For constant generation in Acc

JMP	COND	Register / Program Memory Address

Conditional Jump

RET

Return

TIMER	W	CONT

Timer Control

SLEEP	MODE

Sleep Controls

Section E: REFERENCES

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