INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

Stamp / Signature of the Invigilator

EXAMINATION (Mid Semester)	**SEMESTER (Spring)**

Roll Number									**Section**		**Name**	

Subject Number	C	S	2	1	0	0	2	**Subject Name**	*Switching Circuits and Logic Design*

Department / Center of the Student		**Additional sheets**	

Important Instructions and Guidelines for Students

1. You must occupy your seat as per the Examination Schedule/Sitting Plan.
2. Do not keep mobile phones or any similar electronic gadgets with you even in the switched off mode.
3. Loose papers, class notes, books or any such materials must not be in your possession, even if they are irrelevant to the subject you are taking examination.
4. Data book, codes, graph papers, relevant standard tables/charts or any other materials are allowed only when instructed by the paper-setter.
5. Use of instrument box, pencil box and non-programmable calculator is allowed during the examination. However, exchange of these items or any other papers (including question papers) is not permitted.
6. Write on both sides of the answer script and do not tear off any page. **Use last page(s) of the answer script for rough work.** Report to the invigilator if the answer script has torn or distorted page(s).
7. It is your responsibility to ensure that you have signed the Attendance Sheet. Keep your Admit Card/Identity Card on the desk for checking by the invigilator.
8. You may leave the examination hall for wash room or for drinking water for a very short period. Record your absence from the Examination Hall in the register provided. Smoking and the consumption of any kind of beverages are strictly prohibited inside the Examination Hall.
9. Do not leave the Examination Hall without submitting your answer script to the invigilator. **In any case, you are not allowed to take away the answer script with you.** After the completion of the examination, do not leave the seat until the invigilators collect all the answer scripts.
10. During the examination, either inside or outside the Examination Hall, gathering information from any kind of sources or exchanging information with others or any such attempt will be treated as **'unfair means'**. Do not adopt unfair means and do not indulge in unseemly behavior.

Violation of any of the above instructions may lead to severe punishment.

Signature of the Student

To be filled in by the examiner

Question Number	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**Total**
Marks Obtained											

Marks obtained (in words)	**Signature of the Examiner**	**Signature of the Scrutineer**

CS21002 Switching Circuits and Logic Design

Mid-Semester Test

20–February–2016 | 2:00–4:00pm | Maximum marks: 60

[*Write your answers in the question paper itself. Be brief and precise. Answer all questions.*]

1. Recall that the dual of a Boolean function is obtained by interchanging the AND and OR operations and the constants 0 and 1. For example, the dual of $a+b'(cd'+e)+0$ is $a(b'+(c+d')e)1$. Denote the dual of f by f_d. A Boolean function is called *self-dual* if $f = f_d$.

(a) Using algebraic manipulations, prove that $f(x,y,z) = xy+yz+zx$ is self-dual. **(5)**

Solution $f_d(x,y,z) = (x+y)(y+z)(z+x) = (y+xz)(z+x) = yz+xz+xy+xz = xy+yz+zx = f(x,y,z)$.

(b) Prove that there are exactly $2^{2^{n-1}}$ self-dual Boolean functions in n input variables. **(5)**

Solution First, note that $f_d(x_1,x_2,\ldots,x_n) = [f(x_1',x_2',\ldots,x_n')]'$. This requires the lower half of the truth table of f be the complemented reflection of the upper half of the table. We can fix the upper half in any of the $2^{2^{n-1}}$ ways. The self-duality requirement then fixes the lower half.

2. Consider the Boolean function $g(w,x,y,z) = \sum m(0,1,2,4,5,10,12,13,14,15) + \sum d(6,8)$.

(a) Use the Quine–McCluskey tabulation procedure to find all the prime implicants of g. (No credits will be given if you manually identify the prime implicants from the Karnaugh map of g.) **(10)**

Solution The steps of the tabulation procedure follows.

Index	Init		Round 1		Round 2		Round 3	
0	0	✓	$0,1(z)$	✓	$0,1,4,5(xz)$	*B*	$0,2,4,6,8,10,12,14(wxy)$	*A*
			$0,2(y)$	✓	$0,2,4,6(xy)$	✓		
			$0,4(x)$	✓	$0,2,8,10(wy)$	✓		
			$0,8(w)$	✓	$0,4,8,12(wx)$	✓		
1	1	✓	$1,5(x)$	✓	$2,6,10,14(wx)$	✓		
	2	✓	$2,6(x)$	✓	$4,5,12,13(wz)$	*C*		
	4	✓	$2,10(w)$	✓	$4,6,12,14(wy)$	✓		
	8	✓	$4,5(z)$	✓	$8,10,12,14(xy)$	✓		
			$4,6(y)$	✓				
			$4,12(w)$	✓				
			$8,10(y)$	✓				
			$8,12(x)$	✓				
2	5	✓	$5,13(w)$	✓	$12,13,14,15(yz)$	*D*		
	6	✓	$6,14(w)$	✓				
	10	✓	$10,14(x)$	✓				
	12	✓	$12,13(z)$	✓				
			$12,14(y)$	✓				
3	13	✓	$13,15(y)$	✓				
	14	✓	$14,15(z)$	✓				
4	15	✓						

(b) Draw the prime implicant chart for g, identify the essential prime implicants, and derive a minimum sum-of-products expression for g. **(10)**

Solution The prime implicant chart follows.

	✓ 0	✓ 1	✓ 2	✓ 4	✓ 5	✓ 10	✓ 12	✓ 13	✓ 14	✓ 15
$\rightarrow A = z'$	×		⊗	×		⊗	×		×	
$\rightarrow B = w'y'$	×	⊗		×	×					
$C = xy'$				×	×		×	×		
$\rightarrow D = wx$							×	×	×	⊗

The chart shows that A, B and D are essential prime implicants. Including them covers all the minterms of f. Therefore the minimum SOP expression for g is

$$g(w,x,y,z) = z' + w'y' + wx.$$

3. A transmission system encodes the bit 0 as 0000 and the bit 1 as 1111. This leads to one-error-correcting and two-error-detecting capability. Suppose that noise during the transmission of an encoded bit can introduce errors in at most two bits of the codeword. The potentially noisy four-bit codeword that you receive is denoted by *abcd*. Design a combinational circuit which takes the four received bits as inputs (their complements are not input). The circuit has three output bits f_0, f_1, f_2, where $f_0 = 1$ if and only if 0 was transmitted, $f_1 = 1$ if and only if 1 was transmitted, and $f_2 = 1$ if and only if there were two errors. Your design is required to use as few standard gates (two-input AND, OR, NAND, NOR, XOR and XNOR gates, and NOT gates) as possible. It is possible to design this circuit using only eleven gates. The evaluation of your answer will depend on (correctness and) how many gates you use. Derive the necessary expressions for the three outputs, and draw the gate-level diagram of your circuit. **(10)**

Solution The received bit is 0 if and only if all the received bits are 0 or only one of them is 1. Therefore, we have

$$\begin{aligned} f_0 &= a'b'c'd' + ab'c'd' + a'bc'd' + a'b'cd' + a'b'c'd \\ &= (a'b + ab' + a'b')c'd' + a'b'(c'd' + cd' + c'd) \\ &= (ab)'(c+d)' + (a+b)'(cd)' \\ &= [(ab) + (c+d)]' + [(a+b) + (cd)]' \\ &= \Big[\big((ab) + (c+d)\big)\big((a+b) + (cd)\big)\Big]'. \end{aligned}$$

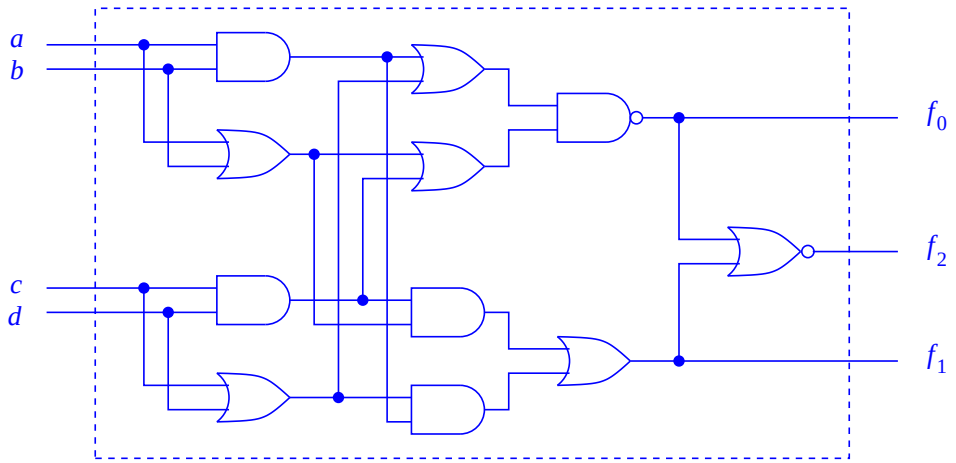
The received bit is 1 if and only if all the received bits are 1 or only one of them is 0. Therefore, we have

$$\begin{aligned} f_1 &= abcd + a'bcd + ab'cd + abc'd + abcd' \\ &= (ab + a'b + ab')cd + ab(cd + c'd + cd') \\ &= (a+b)(cd) + (ab)(c+d). \end{aligned}$$

Finally, we have

$$f_2 = (f_0 + f_1)'.$$

This gives the following circuit with eleven gates.



4. (a) Consider a two-bit comparator circuit which takes two two-bit unsigned integers a and b as input, and outputs two bits g and l. If $a > b$, we have $g = 1$ and $l = 0$. If $a < b$, we have $g = 0$ and $l = 1$. Finally, if $a = b$, we have $g = l = 0$. Derive the expressions for g and l, and write a gate-level Verilog module to implement this two-bit comparator. **(5+5)**

Solution Let $a = (a_1a_0)_2$ and $b = (b_1b_0)_2$. We have $g = 1$ if and only if $(a,b) = (1,0),(2,0),(3,0),(2,1),(3,1),(3,2)$, that is,

$$\begin{aligned} g &= (a_1'a_0 + a_1a_0' + a_1a_0)b_1'b_0' + (a_1a_0' + a_1a_0)b_1'b_0 + (a_1a_0)b_1b_0' \\ &= (a_1 + a_0)(b_1 + b_0)' + a_1b_1'b_0 + a_1a_0b_1b_0'. \end{aligned}$$

Symmetrically, we have

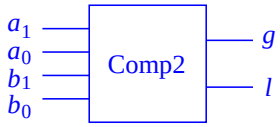
$$l = (b_1 + b_0)(a_1 + a_0)' + b_1a_1'a_0 + b_1b_0a_1a_0'.$$

Based on this, a Verilog module can be written as follows.

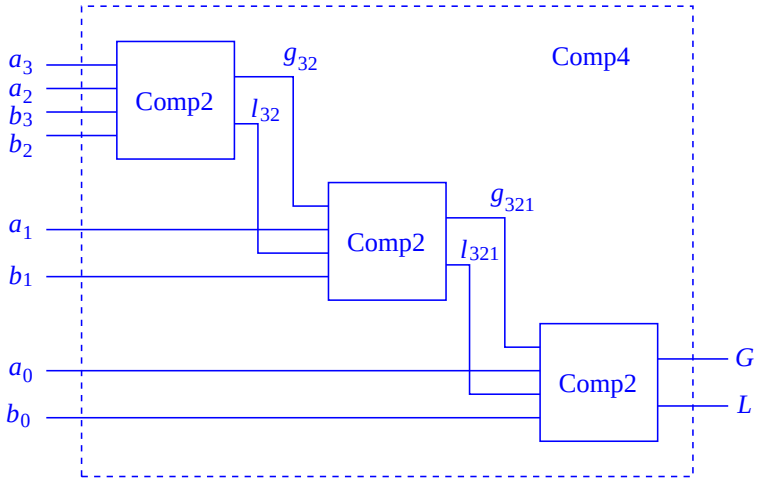
```
module comp2 (g,l,a1,a0,b1,b0);
   output g,l;
   input a1,a0,b1,b0;

   or   (c1,a1,a0), (d1,b1,b0);
   not  (c2,d1), (d2,c1);
   and  (c3,c1,c2), (d3,d1,d2);
   not  (c4,b1), (d4,a1);
   and  (c5,a1,c4,b0), (d5,b1,d4,a0);
   not  (c6,b0), (d6,a0);
   and  (c7,a1,a0,b1,c6), (d7,b1,b0,a1,d6);
   or   (g,c3,c5,c7), (l,d3,d5,d7);
endmodule
```

(b) Your goal is to realize a four-bit comparator. It takes two four-bit unsigned integers $A = (a_3a_2a_1a_0)_2$ and $B = (b_3b_2b_1b_0)_2$ as input, and outputs two bits G and L. If $A > B$, we have $(G,L) = (1,0)$. If $A < B$, we have $(G,L) = (0,1)$. Finally, if $A = B$, we have $(G,L) = (0,0)$. Use three two-bit comparators designed in Part (a) to implement the four-bit comparator. Draw a schematic diagram of your circuit, and write a Verilog module to realize this circuit. **(5+5)**

Solution Let us schematically represent the two-bit comparator of Part (a) as follows.



A four-bit comparator can be constructed from three copies of the two-bit comparator as follows.



This leads to the following Verilog module.

```
module comp4 (G,L,a3,a2,a1,a0,b3,b2,b1,b0);
   output G,L;
   input a3,a2,a1,a0,b3,b2,b1,b0;

   comp2 C32(g32,l32,a3,a2,b3,b2),
         C321(g321,l321,g32,a1,l32,b1),
         C3210(G,L,g321,a0,l321,b0);
endmodule
```