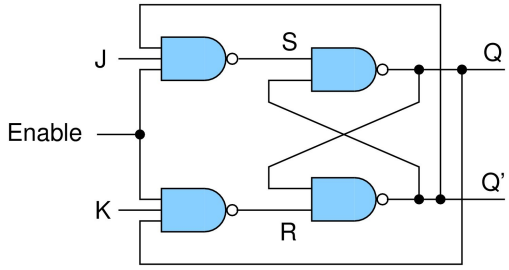
CS29002 SWITCHING LABORATORY
CSE Department, IIT Kharagpur
Spring Semester 2015–16
Module C: Sequential Circuits and Finite State Machines
Assignment 1
Date: 07–March–2016

This assignment deals with the design of flip-flops. In the class, we have seen how the basic SR latch can be converted to a D latch and how two D latches can be connected in the master-slave fashion so as to give an edge-triggered D flip-flop. In this assignment, you build JK latches and JK flip-flops.

Part 1: Design a JK latch with an enable input. The following figure demonstrates an implementation using four NAND gates. This JK latch is built from the SR latch in such a way that when both J and K inputs are 1, the state is toggled. For other inputs, the operation is the same as in the SR latch. Your design should use four NOR gates only.



Part 2: Make two copies (master and slave) of the basic JK latch designed in Part 1. Supply the clock (and its complement) to the enable inputs of the latches so that you get the functionality of a positive edge-triggered JK flip-flop. Verify the truth table of the flip-flop. Use a manual clock.

Part 3: Convert the JK flip-flop designed in Part 2 to a T flip-flop. Supply a square wave at its clock input. Verify, using an oscilloscope, how the T flip-flop divides the frequency of the input clock pulse train by two.