CS21002 Switching Circuits and Logic Design, Spring 2015–2016

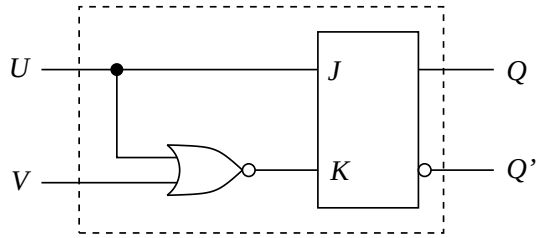
Class Test 2

15–April–2016 6:00–7:00pm Maximum marks: 20

Roll no: _____ **Name:** _____

[*Write your answers in the question paper itself. Be brief and precise. Answer all questions.*]

1. Consider a UV flip-flop (the dotted box) designed from a JK flip-flop and a NOR gate as shown below.



(a) Describe the state transitions of the UV flip-flop for the four input combinations. Also draw the excitation table for the UV flip-flop. **(5)**

Solution

Transition table

U	V	J	K	$Q(t+1)$
0	0	0	1	0
0	1	0	0	$Q(t)$
1	0	1	0	1
1	1	1	0	1

Excitation table

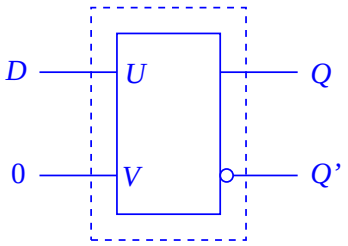
$Q(t)$	$Q(t+1)$	UV
0	0	$0X$
0	1	$1X$
1	0	00
1	1	$01/10/11$

(b) You are given only one UV flip-flop. Realize a D flip-flop. **(5)**

Solution We have the following table for state transition as a function of the D-input.

D	$Q(t)$	$Q(t+1)$	UV
0	0	0	$0X$
0	1	0	00
1	0	1	$1X$
1	1	1	$01/10/11$

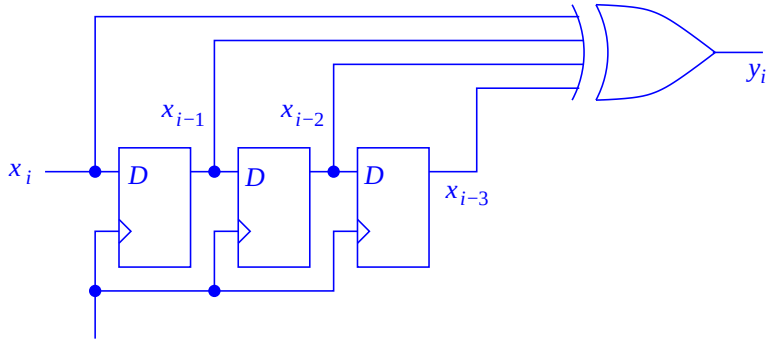
The last line is problematic. Ignoring the 01, we write this as $1X$. This enables us to take $U = D$ and $V = 0$.



2. Design a synchronous sequential circuit that takes a one-bit stream $x_0x_1x_2\ldots$ as input, and outputs a one-bit stream $y_0y_1y_2\ldots$. The i-th output bit y_i is 1 if and only if the four most recently read input bits $x_{i-3}x_{i-2}x_{i-1}x_i$ have odd parity. Here is an example. At the beginning of the input, four bits are not read. Assume that the missing bits are 0 (that is, $x_{-3} = x_{-2} = x_{-1} = 0$). **(5)**

Input: 0100110100111010…
Output: 0111000101001110…

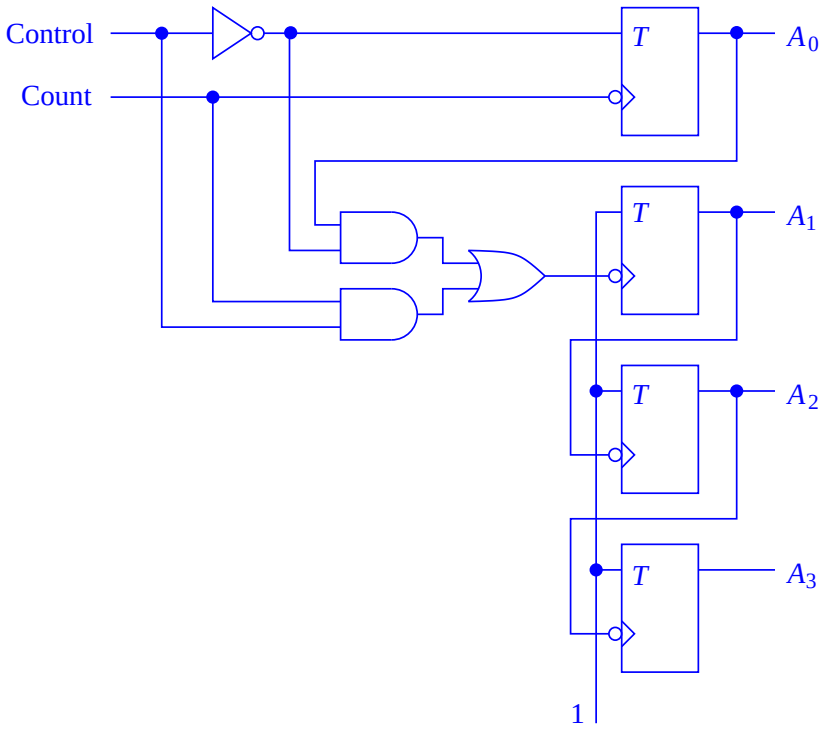
Solution The easiest design is to use a shift register. The last three bits need to be remembered, so a 3-bit register suffices. The register should be initialized to 000.



Note: The above circuit is a Mealy machine that assumes that the output is read immediately before the active edge of the clock pulse, that is, immediately before the state transition occurs. If you read the output *after* the state transition, a 4-bit shift register is necessary. Now, it is a Moore machine, so the output remains constant between two state transitions.

3. Design a 4-bit binary ripple counter (asynchronous) that has one count-enable input and one control input. If the control input is 0, the counter increments by 1 modulo 16. If the control input is 1, the counter increments by 2 modulo 16. Use negative-edge triggered T flip-flops. The count-enable input is (negative) edge-sensitive, whereas the control input is level-sensitive. **(5)**

Solution



For leftover answers and rough work