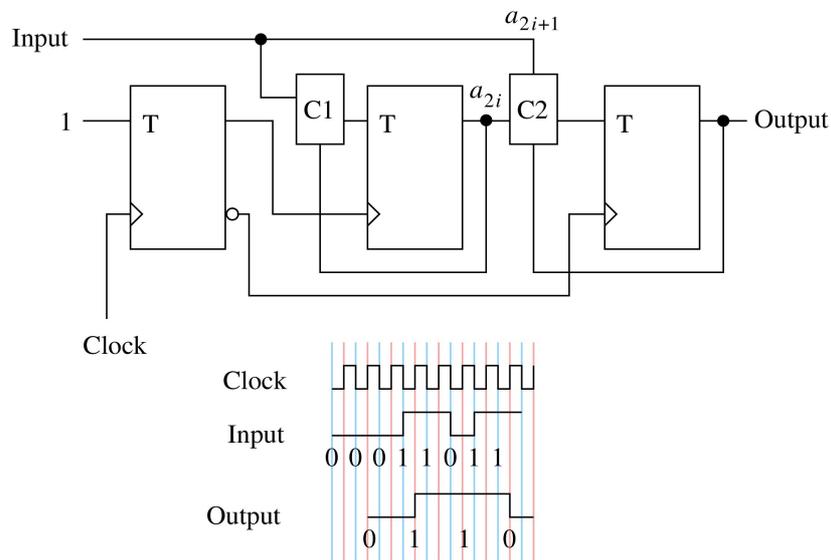

CS29002 SWITCHING LABORATORY
CSE Department, IIT Kharagpur
Spring Semester 2015–16
Laboratory test: Group member with larger roll number
Date: 12–April–2016 (4:30pm – 6:30pm)

Design a synchronous sequential circuit using three T flip-flops, that works as follows. The circuit takes a one-bit input sequence $a_0 a_1 a_2 a_3 \dots a_{2i} a_{2i+1} \dots$, and processes two bits from the input at a time. It outputs a single bit at every alternate clock pulse. The i -th output bit is 0 if and only if the two input bits a_{2i} and a_{2i+1} are equal. Here is an example:

Input: 0 0 0 1 1 0 1 1 ...
 Output: 0 1 1 0 ...

Use the first T flip-flop as a frequency divider (divide-by-2). Its outputs should feed the clocks of the other flip-flops. The second flip-flop remembers the input bits with even indices. The third flip-flop prepares the output using the bit stored in the second flip-flop and the next odd-indexed bit in the input. This idea is described in the following figure which assumes that the T flip-flops are positive-edge triggered. Assume that the input changes when the clock remains inactive (well before the active edge of the clock pulse). The output is measured from the state of the third flip-flop. This is a Moore machine, and its output remains constant for two clock pulses. At the beginning, the state of the frequency divider flip-flop is reset to 0. Your task is to design the combinational circuits C1 and C2.



Use a manual clock to demonstrate the operation of your circuit.
