
CS29002 SWITCHING LABORATORY
CSE Department, IIT Kharagpur
Spring Semester 2015–16
Module C: Sequential circuits and finite state machines
Assignment 2
Date: 21–March–2016

In this assignment, you design synchronous sequential circuits to solve the following two parts.

1. Design a modulo-9 synchronous binary counter using JK flip-flops. The counter counts in the sequence 0,1,2,...,8, and then back to 0. The modulo-9 increment happens at the active edge of each clock pulse.
2. Design a circuit that will take a serial bit stream as input, synchronized with a clock, and will output a 1 whenever the pattern (possibly overlapping) 01001 is encountered. Use D flip-flops.

In this assignment, you do not need to realize flip-flops using logic gates. Use built-in flip-flops from IC chips available in the lab. For example, you may use the CMOS chips 4013 (D flip-flops) and 4027 (JK flip-flops).

Both the machines are to be designed as Moore machines. You need to reset the state to a start state before the input appears. Use a manual clock in both the circuits. In the second circuit, change the input any time when the clock remains inactive, and read the output after the active edge of each clock pulse.