CS29002 SWITCHING LABORATORY
CSE Department, IIT Kharagpur
Spring Semester 2015–16
Module B: CMOS Characteristics
Assignment 1
Date: 18–Jan–2016

In this experiment, you study the characteristics of a CMOS inverter circuit. Carry out the following parts.

(a) Realize an inverter using the IC chip 4007. This chip supplies three nMOS and three pMOS transistors. You need only one pair for implementing one inverter circuit.

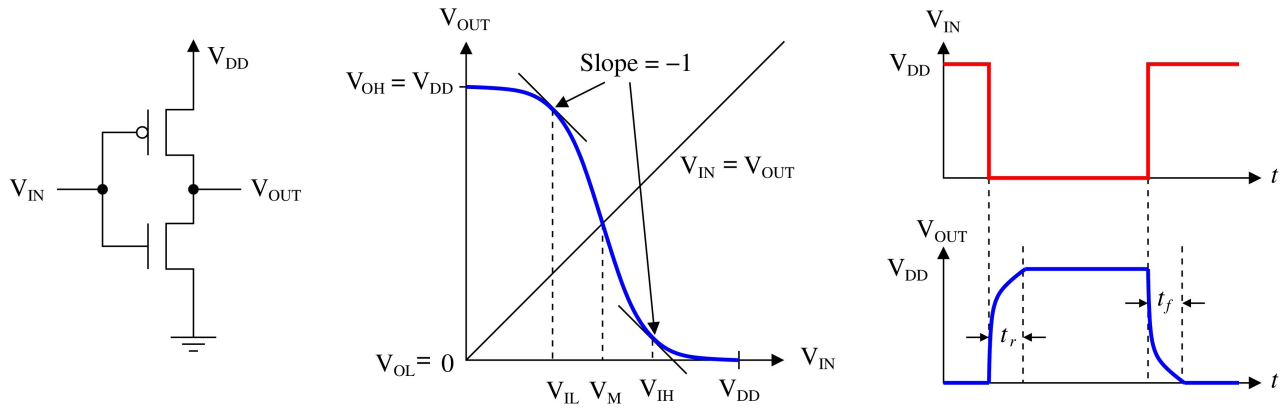
(b) Study the transfer characteristics of the inverter by varying the input voltage in steps of 0.5V and measuring both the input and output voltages with the help of an oscilloscope. You may have to increase the measurement resolution (like in steps of 0.1V) at the transition zone of the curve (see Part (b) of the figure below). Plot the readings on a graph paper, and obtain the high and low noise margins for CMOS gates (noise margins are defined below).

(c) Display the transfer characteristics by applying a triangular signal at the input (using the *X*-*Y* mode of the oscilloscope). Plot the hysteresis loop on a graph paper.

(d) Realize three-input NAND and NOR gates using the three pairs of transistors in the chip 4007. Recall that you need to connect the nMOS transistors in series and the pMOS transistors in parallel for realizing a NAND gate. For designing a NOR gate, do the opposite. Verify the truth tables, and measure the rise and fall times by switching the inputs between 000 and 111 (short the three inputs and supply a square wave at the common input).

Background Information

The circuit of a CMOS inverter is shown in Part (a) of the following figure.



(a) (b) (c)

Part (b) of the figure shows the typical DC characteristics of a CMOS inverter. The input-high and input-low voltages are usually taken to be those input voltages at which the slope of the curve is –1. The output-high and output-low voltages are V_{DD} and 0. The high and low noise margins are defined as:

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH},$$
$$NM_L = V_{IL} - V_{OL} = V_{IL}.$$

Part (c) shows the typical AC characteristics of the inverter in response to a square wave. The rise and fall delays are caused by external and internal (parasitic) capacitors. If you apply a triangular wave to the input of the inverter, these delays cause the output voltage to exhibit a hysteresis loop.